VPX580

Zynq UltraScale+ FPGA, Dual FMC Carrier, 6U VPX

Key Features

- Xilinx UltraScale+ XCZU19EG FPGA
- 8 GB of 64-bit wide DDR-4 Memory (single bank) with ECC
- Dual FMC sites on a 6U VPX
- MPSoC with block RAM and UltraRAM
- Health Management through dedicated Processor

Benefits

- Electrical, mechanical, software, and system-level expertise in house
- Full system supply from industry leader
- AS9100 and ISO9001 certified company

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VPX580

The VPX580 is a 6U VPX FPGA Carrier with dual FMC (VITA 57) interfaces. The unit has an on-board, re-configurable FPGA which interfaces directly to the VPX P1 connector, FMC DP0-9 and all FMC LA/HA/HB pairs.

The FPGA has interface to a single DDR4 memory channel (64-bit wide). This allows for large buffer sizes to be stored during processing as well as for queuing the data to the host.

The VPX580 is based on Xilinx UltraScale+ XCZU19EG MPSoC FPGA with dual FMC sites.

The FPGA has 1968 DSP Slices and 1143K logic cells. The XCZU19EG includes a quad-core ARM processor.

The module has on board 64 GB of Flash, 128 MB of boot flash and an SD Card as an option.

Block Diagram

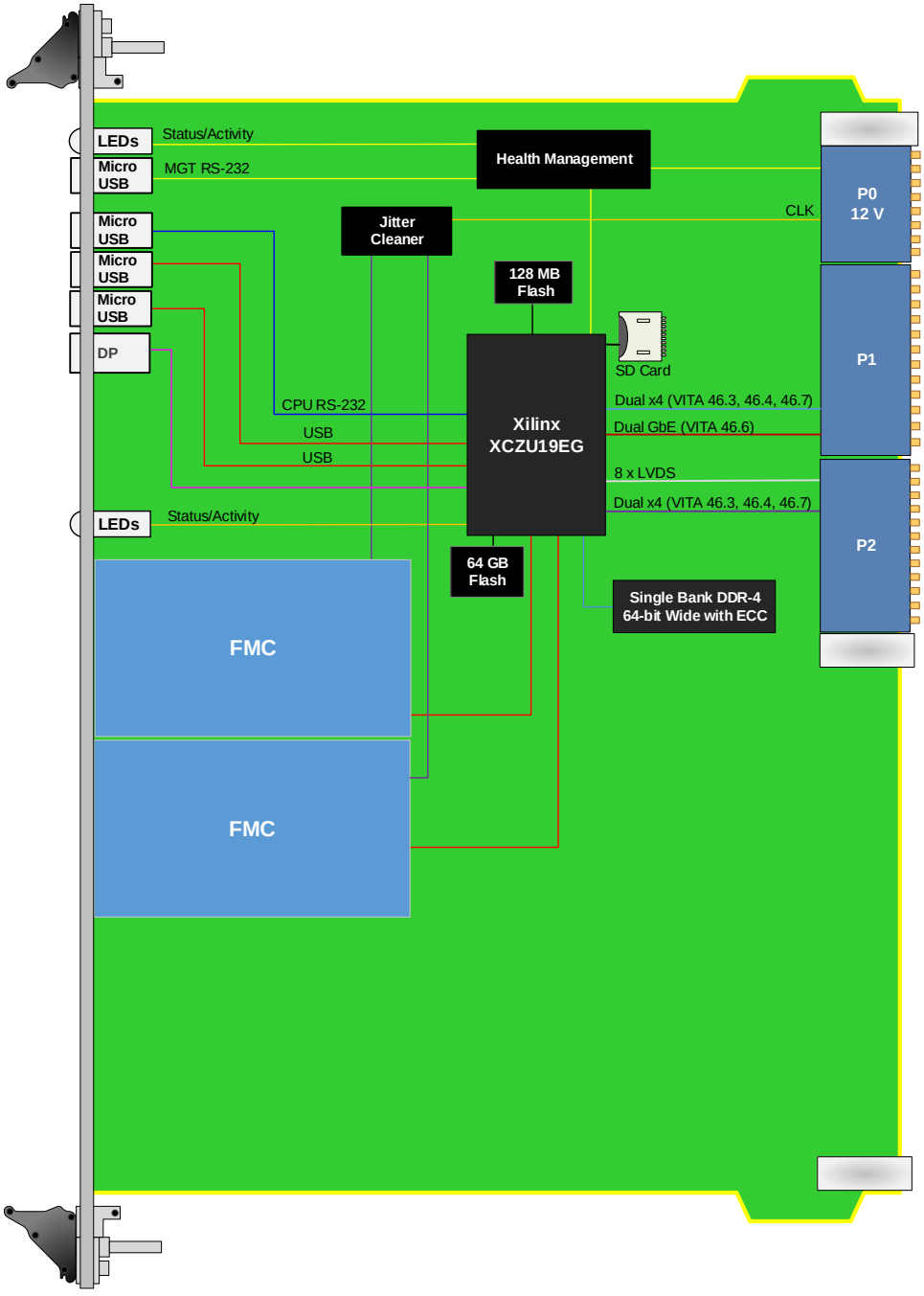

Figure 1: VPX580 Block Diagram

Front Panel

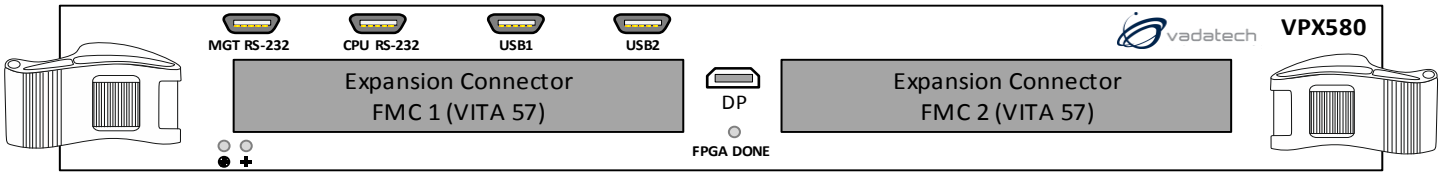

Figure 2: VPX580 Front Panel

Reference Design

VadaTech provides an extensive range of Xilinx based FPGA products. The FPGA products are in two categories; FPGA boards with FMC carriers and FPGA products with high speed ADC and DACs. The FPGA products are designed in various architectures such as AMC modules, PCIe cards and Open VPX.

VadaTech provides a reference design implementation for our FPGAs complete with VHDL source code, documentation and configuration binaries. The reference design focuses on the I/O ring of the FPGA to demonstrate low-level operation of the interconnections between the FPGA and other circuits on the board and/or backplane. It is designed to prove out the hardware for early prototyping, engineering/factory diagnostics and customer acceptance of the hardware, but it does not strive to implement a particular end application. The reference VHDL reduces customer time to develop custom applications, as the code can be easily adapted to meet customer's application requirements.

The reference design allows you to test and validate the following functionality (where supported by the hardware):

- Base and Fabric channels
- Clocks
- Data transfers
- Memory
- User defined LEDs

Xilinx provides Vivado Design Suite for developing applications on Xilinx based FPGAs. VadaTech provides reference VHDL developed using the Vivado Design Suite for testing basic hardware functionality. The reference VHDL is provided royalty free to use and modify on VadaTech products, so can be used within applications at no additional cost. However, customers are restricted from redistributing the reference code and from use of this code for any other purpose (e.g. it should not be used on non-VadaTech hardware).

The reference VHDL is shipped in one or more files based on a number of ordering options. Not all ordering options have an impact on the FPGA and a new FPGA image is created for those options that have direct impact on the FPGA. Use the correct reference image to test your hardware. For more information, refer to the FPGA reference design manual for your device which can accessed from customer support site along with the reference images.

Supported Software

- Default FPGA image stored in flash memory
- Linux BSP
- Build Scripts
- Device Driver
- Reference application projects for other ordering options

The user may need to develop their own FPGA code or adapt VadaTech reference code to meet their application requirements. The supplied pre-compiled images may make use of hardware evaluation licenses, where necessary, instead of full licenses. This is because VadaTech does not provide licenses for the Vivado tool or Xilinx IP cores, so please contact Xilinx where these are required.

Xilinx also provides System Generator tools for developing Digital Signal Processing (DSP) applications.

See the following links:

Xilinx Vivado Design Suite, Xilinx System Generator for DSP.

Specifications

Architecture		
Physical	**Dimensions**	6U, 1" pitch
Type	**FPGA**	Xilinx Zynq UltraScale+ with Dual FMC sites
Configuration		
Power		35 W FPGA load dependent (without FMC)
Front Panel	**Interface Connectors**	Dual FMC Slots
	Micro USB	RS-232 from FPGA and RS-232 from Health Management
		USB1, USB2
		Display Port
	LEDs	User defined by the FPGA and Health Management
VPX Interfaces	**Slot Profiles**	See ordering options
	Rear IO	CLK on P0
		Dual x4 fabric (VITA 46.3, 46.4, 46.7) on P1
		Dual GbE (VITA 46.6) on P1
		Dual x4 fabric (VITA 46.3, 46.4, 46.7) on P2
		8 x LVDS on P2
Software Support	**Operating System**	Linux
Other		
MTBF	MIL Hand book 217-F@ TBD hrs	
Certifications	Designed to meet FCC, CE and UL certifications, where applicable	
Standards	VadaTech is certified to both the ISO9001:2000 and AS9100B:2004 standards	
Warranty	Two (2) years	

INTEGRATION SERVICES AND APPLICATION-READY PLATFORMS

VadaTech has a full ecosystem of OpenVPX, ATCA and MTCA products including chassis platforms, shelf managers, AMC modules, Switch and Payload Boards, Rear Transition Modules (RTMs), Power Modules, and more. The company also offers integration services as well as pre-configured Application-Ready Platforms. Please contact VadaTech Sales for more information.

Ordering Options

VPX580 – 0BC-DEF-GHJ

	D = FPGA Speed	G = Applicable Slot Profiles
	1 = Reserved 2 = High 3 = Highest	0 = 5 HP
B = Expansion Plane (P2)	**E = Clock Holdover Stability**	**H = Environmental**
0 = Not routed 1 = Routed	0 = Standard (XO) 1 = Stratum-3 (TCXO)	See Environmental Specification Table below
C = SD Card	**F = PCIe Option (P1) for Data Port 1/2**	**J = Conformal Coating**
0 = None 1 = 32 GB	0 = None 1 = PCIe/None 2 = None/PCIe 3 = PCIe/PCIe	0 = None 1 = Humiseal 1A33 Polyurethane 2 = Humiseal 1B31 Acrylic

Environmental Specification

	Air Cooled		Conduction Cooled		
Option H	**H = 0**	**H = 1**	**H = 2**	**H = 3**	**H = 4**
Operating Temperature	AC1* (0°C to +55°C)	AC3* (-40°C to +70°C)	CC1* (0°C to +55°C)	CC3* (-40°C to +70°C)	CC4* (-40°C to +85°C)
Storage Temperature	C1* (-40°C to +85°C)	C3* (-50°C to +100°C)	C1* (-40°C to +85°C)	C3* (-50°C to +100°C)	C3* (-50°C to +100°C)
Operating Vibration	V2* (0.04 g2/Hz max)	V2* (0.04 g2/Hz max)	V3* (0.1 g2/Hz max)	V3* (0.1 g2/Hz max)	V3 (0.1 g2/Hz max)
Storage Vibration	OS1* (20g)	OS1* (20g)	OS2* (40g)	OS2* (40g)	OS2* (40g)
Humidity	95% non-condensing	95% non-condensing	95% non-condensing	95% non-condensing	95% non-condensing

Notes: *Nomenclature per ANSI/VITA 47. Contact local sales office for conduction cooled (H = 2, 3, 4).

Related Products

VPX592

- 3U FPGA carrier for FPGA Mezzanine Card (FMC) per VITA 46 and VITA 57
- Xilinx Kintex UltraScale™ XCKU115 FPGA
- High-performance clock jitter cleaner

VPX599

- Xilinx Kintex UltraScale™ XCKU115 FPGA
- Dual ADC @ 6.4 GSPS 12-bits
- Dual DAC @ 12 GSPS 16-bits (AD9162 or AD9164)

Contact

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