VPX337

VPX Time and Frequency with Onboard GPS and IRIG

VPX337

Key Features

- GPS/PTP (1588)/IRIG/NTP Grand Master Clock
- Synchronous Ethernet
- Three arbitrary frequency disciplined clocks
- IRIG AM decoder input/IRIG DCLS input/output
- Dual PCIe Gen2 x4 or Dual 10GbE
- Dual 1000Base-X (one can mux to front RJ-45)
- 100ns precision UTC timestamps, system status and GPS positions via PCIe
- TSIP data Broadcast/Multicast/Unicast via Ethernet w/ bonding/failover
- Battery or SuperCap Almanac/Ephemeris/Last position back-up
- 1PPS PCIe interrupt, time events, time trigger for overall system/software synchronization
- Holds over clocks/1PPS using OCXO
- GPS NMEA serial port
- Health Management through dedicated Processor

Benefits

- Complete GPS/PTP (1588)/IRIG/NTP solution
- Flexible allocation to backplane clock signals
- Grand-Master Clock/Clock Bridge capability
- Electrical, mechanical, software, and system-level expertise in house
- Full system supply from industry leader
- AS9100 and ISO9001 certified company

OpenVPX™

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THE POWER OF VISION

VPX337

The VPX337 provides a complete, feature-rich, GPS/PTP (1588)/IRIG/NTP bus-level timing solution to a VPX system, with exceptional flexibility.

The onboard GPS receiver, or 1PPS, or Inter-Range Instrumentation Group (IRIG) input, is used to discipline the local oscillator and cancel out any oscillator drift or aging. Precision UTC timestamps and GPS location/time/status are all made available via PCIe registers to the host CPU/application. Time trigger output and time event interrupts synchronized to GPS UTC are available under host control. GPS location/time/status data is Broadcast/Unicast output via backplane Ethernet with selectable bonding/failover behavior.

The board can demodulate IRIG Amplitude Modulated (AM) signals and receive/transmit IRIG DC Level Shift (DCLS) signals. The disciplined clock, 1PPS, divided-down clocks, IRIG DCLS, and time trigger may be output in any combination to the dual clock options on the VPX backplane channels (P0_REF_CLK+/- and/or P0_AUX_CLK+/-). It also acts as a Grand-Master Clock/Clock Bridge between GPS/PTP (1588)/IRIG/NTP to provide enhanced flexibility to your system design. The board also supports Synchronous Ethernet (SyncE) to eliminate clock drift at the Ethernet PHY level.

A back-up battery or SuperCap provides non-volatile storage of the Almanac, Ephemeris and last position data to enable rapid “warm start” re-acquisition, usually within 35 seconds.

The module’s console is available via front serial or SSH via Ethernet. Locking/holdover status is also available via IPMI sensors. A secondary serial port enables GPS NMEA data in/out.

The module interfaces to the backplane via multiple options. Dual GbE to Ports 14 and 15 as dual PCIe x4 to Ports 0-7 or as 10GbE (XAUI) to Ports 0-7. The module can drive the dual VPX clocks that are on the P0.

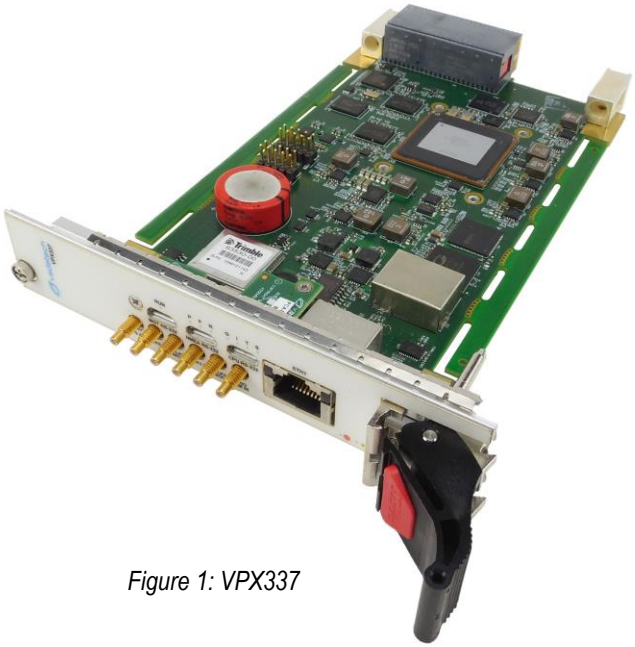

Figure 1: VPX337

Block Diagram

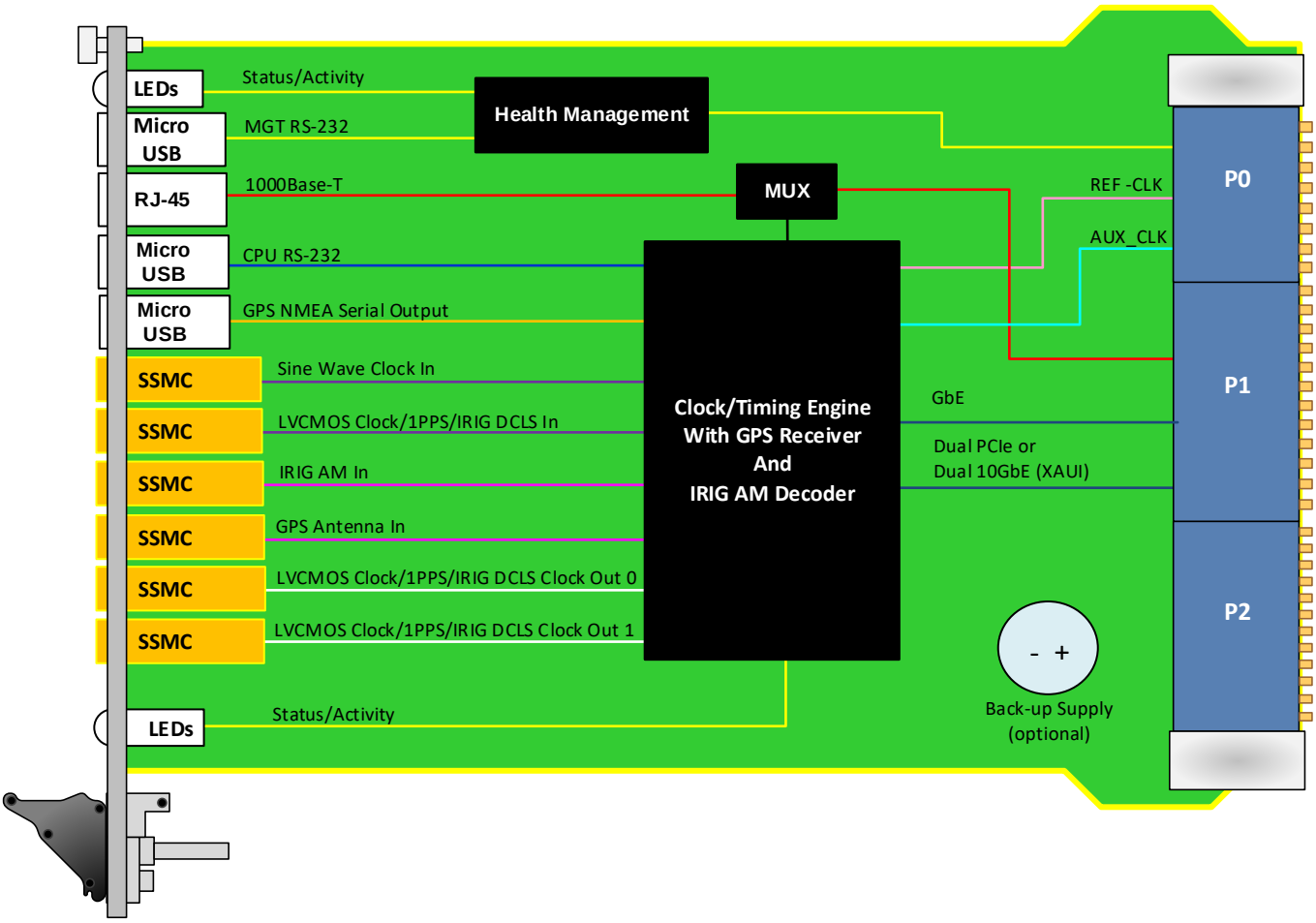

Figure 2: VPX337 Functional Block Diagram

Pinout Block Diagram

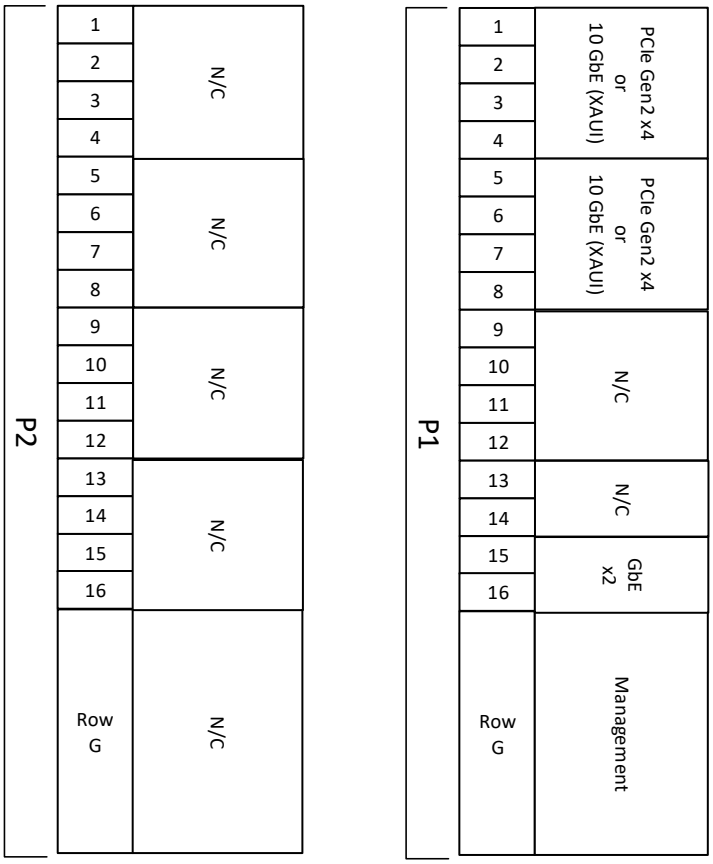

Figure 3: VPX337 Pinout Block Diagram

GPS Receiver

The VPX337 includes an onboard GPS receiver which is capable of obtaining precise timing information from the GPS satellite constellation via a +3.3V active GPS antenna. (The module provides the power to antenna.) The antenna connection includes short/open detection circuitry and this status is provided via sensors. The GPS receiver provides NMEA serial data out the front panel for interfacing to other equipment. The receiver provides the clock/timing engine with location, velocity, time, and status information as well as a 1PPS pulse. The clock/timing engine integrates this information together to create accurate time/clock references to the rest of the system.

IRIG AM Demodulator

The VPX337 includes an onboard IRIG Amplitude Modulated (AM) signal demodulator. The output of this demodulator includes time code data as well as 1PPS and reference frequency signals. The clock/timing engine integrates this information together to create accurate time/clock references to the rest of the system.

Ethernet Ports with PTP (IEEE1588), NTP and Synchronous Ethernet

The VPX337 includes two 1000Base-X ports to the backplane base fabric (one of which can be re-directed to a 1000Base-T port on the front panel). It also includes two optional XAUI (10GbE) ports to the backplane fat pipes fabric. Any of these ports can be declared a Synchronous Ethernet (SyncE) master (or some other clock reference can be the master internally) and the other ports can be slaved to match the clock of the master port; this eliminates drift within the Ethernet PHY layer of the system when used in conjunction with other equipment that supports SyncE. All of these ports can also participate in PTP (IEEE1588) or NTP time synchronization protocols. The VPX337 can be a PTP/NTP master or a PTP/NTP slave and can bridge PTP/NTP to/from other timing protocols. The board can also broadcast/multicast/unicast the GPS Receiver's TSIP data (location/velocity/approximate time/status) to these ports.

Front Panel Clock I/O

The VPX337 can accept a sine wave clock in the range of 10 MHz to 3 GHz for use in disciplining the onboard clock synthesizer. This sine wave clock can also be routed to other clock outputs if the frequency is kept within a more limited range of 10 MHz to 350 MHz.

An LVCMOS clock input is also provided which can be used to input a clock or a 1PPS signal in the range of DC to 315 MHz. This port can also be used to input IRIG DCLS time code as an alternative to the IRIG AM Demodulator input.

Two LVCMOS clock outputs are provided which can output many different clocks, 1PPS signals, and/or IRIG DCLS signals from within the unit via an onboard cross-point switch matrix used for routing. These outputs can be used for signals ranging from DC to 200 MHz.

Backplane Clock I/O

The VPX337 connects to the Dual VPX clock on P0 and can input/output clocks, 1PPS signals, and/or IRIG DCLS signals using the onboard cross-point switch matrix used for routing. These inputs/outputs can be used for signals ranging from DC to 350 MHz.

Clock Disciplining and Arbitrary Frequency Synthesis

The VPX337 uses an OCXO (Oven Controlled Crystal Oscillator) and a high-quality network synchronizer PLL to create a disciplined clock and 1PPS pulse from the GPS/IRIG/1PPS input. The disciplined clock can be any arbitrary frequency up to the limits of the outputs as described above. The clock and 1PPS pulse hold over if the input reference is lost to avoid disruption of the downstream clients depending on them.

The board also supports two additional disciplined clocks which can be used to clean up arbitrary references and output arbitrary frequencies. These can also be slaved to the GPS/IRIG/1PPS input as well in case all three output clocks are desired to be derived from a common reference. The OCXO provides exceptional stability during holdover due to the way the oven maintains the crystal within its optimal temperature zone of operation.

PCIe Precision Timestamping Engine

The VPX337 is a complete bus-level timing solution. It maintains precision timestamps using the GPS-disciplined oscillator and can provide these timestamps on demand via PCIe registers to an external host CPU (Processor module). Additional data is also available such as the GPS location/velocity/status information. Enhanced features such as 1PPS interrupts, time event interrupts, and time trigger output signal are also enabled under software control from the customer's application running on the host CPU.

Dual-Core CPU/Console

The VPX337 uses a high-performance dual-core CPU running embedded Linux to host the VadaTech clock/timing software. The CPU console can be accessed via the front panel serial port or via SSH using any of the Ethernet ports. The software/firmware is upgradable in the field using SCP protocol to transfer the field upgrade package to the board for execution.

Specifications

Architecture		
Physical	**Dimensions**	3U, 1" pitch
Standards		
VPX	**Type**	VITA 46.x
VPX	**Type**	VITA 65 OpenVPX
Module Management	**IPMI**	IPMI v2.0
Configuration		
Power	**VPX337**	~7W
Front Panel	**SSMC**	SSMC connector for GPS Antenna, SSMC connector for IRIG AM in, x4 SSMC connectors for clocks in/out
	Micro USB	x3 Micro USB for Serial Interface
		RJ-45 for GbE
	LEDs	IPMI management control, payload power, power good, reset, etc.
VPX Interfaces	**Slot Profiles**	See Ordering Options
	Rear IO	GbE Muxed onto P1
		PCIe or 10GbE on P1
Other		
MTBF	MIL Hand book 217-F@ TBD hrs	
Certifications	Designed to meet FCC, CE and UL certifications, where applicable	
Standards	VadaTech is certified to both the ISO9001:2015 and AS9100D standards	
Warranty	Two (2) years, see VadaTech Terms and Conditions	

INTEGRATION SERVICES AND APPLICATION-READY PLATFORMS

VadaTech has a full ecosystem of OpenVPX, ATCA and MTCA products including chassis platforms, shelf managers, AMC modules, Switch and Payload Boards, Rear Transition Modules (RTMs), Power Modules, and more. The company also offers integration services as well as pre-configured Application-Ready Platforms. Please contact VadaTech Sales for more information.

Ordering Options

VPX337 – A0C-0E0-0HJ

A = GPS/RTC Back-up Supplies		
0 = No back-up supplies 1 = Lithium battery 2 = SuperCap 3 = Lithium battery and SuperCap		
	E = Fabric on P1*	**H = Environmental**
	0 = Dual 10GbE 1 = PCe on 0-3 and 10GbE on 4-7 2 = Dual PCIe Ports 0-7 3 = Reserved 4 = Reserved	See Environmental Specification
C = VPX Connector Type		**J = Conformal Coating**
0 = Standard 50u Gold Rugged 1 = KVPX Connectors		0 = No coating 1 = Humiseal 1A33 Polyurethane 2 = Humiseal 1B31 Acrylic

Notes: *Customers could order with option of having no backplane connection. Please contact VadaTech Sales.

Environmental Specification

	Air Cooled		Conduction Cooled		
Option H	**H = 0**	**H = 1**	**H = 2**	**H = 3**	**H = 4**
Operating Temperature	AC1* (0°C to +55°C)	AC3* (-40°C to +70°C)	CC1* (0°C to +55°C)	CC3* (-40°C to +70°C)	CC4* (-40°C to +85°C)
Storage Temperature	C1* (-40°C to +85°C)	C3* (-50°C to +100°C)	C1* (-40°C to +85°C)	C3* (-50°C to +100°C)	C3* (-50°C to +100°C)
Operating Vibration	V2* (0.04 g2/Hz max)	V2* (0.04 g2/Hz max)	V3* (0.1 g2/Hz max)	V3* (0.1 g2/Hz max)	V3 (0.1 g2/Hz max)
Storage Vibration	OS1* (20g)	OS1* (20g)	OS2* (40g)	OS2* (40g)	OS2* (40g)
Humidity	95% non-condensing	95% non-condensing	95% non-condensing	95% non-condensing	95% non-condensing

Notes: *Nomenclature per ANSI/VITA 47. Contact local sales office for conduction cooled (H = 2, 3, 4).

Related Products

VPX004

- Unified 1 GHz quad-core CPU for, Shelf Manager, and Fabric management
- 1GbE base switch with dual 100/1000/10G uplink
- Full Layer 3 managed Ethernet switch

VPX754

- 3U VPX module Intel 5th Generation Xeon D-1577, D-1548 or D-1520 (Broadwell) SoC
- PCIe Gen3 dual x4 or single x8
- Front-panel video out via micro HDMI

VTX870

- OpenVPX benchtop development platform
- Up to five 3U VPX payload slots
- Compatible with 0.8-inch, 0.85-inch and 1.0-inch modules

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