AMC Quad Channel ADC

AMC500

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KEY FEATURES

- Four channel ADC
- 130 to 200 MSPS @ 16-bit resolution
- Clock in/out configurable by software
- Trig in/out configurable by software
- PCIe x4, SRIO and/or GbE (FPGA programmable)
- Altera Stratix II GX FPGA (EPS2SGX90 or EPS2SGX130)
- Option for 512MB/1GB of DDR-II with ECC
- Option for 72-Mbit QDR-II SRAM
- AMC.1, AMC.2 and AMC.4 compliant (FPGA programmable)
- RoHS compliant
- OS support for:
  - Linux
  - Windows
  - Solaris
  - VxWorks

The AMC500 is a Quad ADC (Analog to Digital Converter) module compliant to the AMC.1*, AMC.2 and AMC.4 specification. The unit has an on-board, re-configurable FPGA which interfaces directly to the GbE, PCIe and/or SRIO bus. The FPGA has an interface to the DDR-II memory with ECC. The memory bus runs at 533Mhz. This allows for large buffer sizes to be stored during processing as well as for queuing the data to the host. The AMC500 also has an option for two 36-Mbit QDR-II SRAM devices.

The AMC500 allows for external clocking as well as internal clocking. The external clock goes through an on-board PLL for buffering and multiplying. The AMC500 has a Trig in/out signal.

Each input/output is via an SMA style connector and each of the ADC inputs are isolated via an on-board RF transformer with 50 Ohm termination.

The FPGA interfaces directly to the AMC per AMC.1, AMC.2 and/or AMC.4. These interfaces allow customers to use soft-core to interface to the host with multiple protocols*.

VadaTech can modify this product to meet special customer requirements without NRE (minimum order placement is required).

*The default configuration in the flash is AMC.1.

AdvancedMC™

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SPECIFICATIONS

Architecture		
Physical	**Dimensions**	Single-width, Mid-Height (with Full-Height option)
		Width: 2.89 in. (73.5 mm)
		Depth: 7.11 in. (180.6 mm)
Type	**AMC ADC**	Quad ADC
		16-bit resolution per port
		External clock with Trig in/out
		DDR-II as well as QDR-II
Standards		
AMC	**Type**	AMC.1, AMC.2 and/or AMC.4 (FPGA programmable)
Module Management	**IPMI**	IPMI Version 2.0
PCIe	**Lanes**	x4
SRIO	**Lanes**	x4
Ethernet	**GbE**	1000-BaseBX
Configuration		
Power	**AMC500**	TBD (estimated 6W)
Environmental	**Temperature**	Operating Temperature: 0° to 65° C (Air flow requirement is to be greater than 400 LFM)
		Storage Temperature: -40° to +90° C
	Vibration	1G, 5-500Hz each axis
	Shock	30Gs each axis
	Relative Humidity	5 to 95 percent, non-condensing
Front Panel	**Interface Connectors**	Six SMA style
	LEDs	IPMI Management Control
		Eight user defined LED
	Mechanical	Hot Swap Ejector Handle
Software Support	**Operating Systems**	Linux, Windows, Solaris and VxWorks
Other		
MTBF	MIL Spec 217-F > TBD.	
Certifications	Designed to meet FCC, CE and UL certifications where applicable	
Standards	VadaTech is certified to both the ISO9001:2000 and AS9100B:2004 standards	
Compliance	RoHS and NEBS	
Warranty	Two (2) years.	
Trademarks and Logos	The VadaTech logo is a registered trademark of VadaTech, Inc. Other registered trademarks are the property of their respective owners. AdvancedMC™ and the AdvancedTCA™ logo are trademarks of the PCI Industrial Computers Manufacturers Group. All rights reserved. Specification subject to change without notice.	

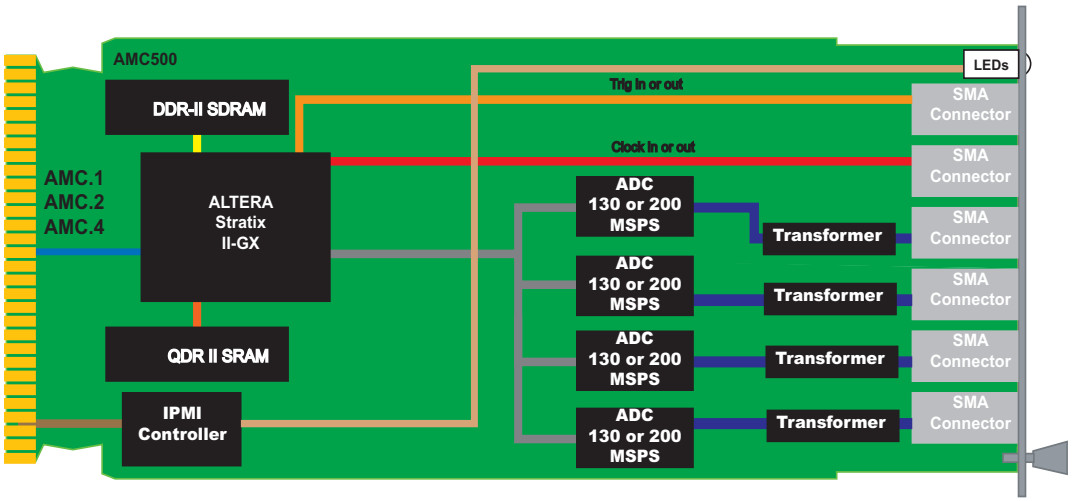

FIGURE 1. AMC500 Functional Block Diagram

ORDERING OPTIONS

AMC500 - ABC - DEF - 00J

A = DDR-II Memory

1 = None
2 = 512MB
3 = 1GB
4 = Reserved

A = QDR-II Memory

1 = None
2 = 2x1x36 Mbit
3 = Reserved

C = Front Panel

1 = Reserved
2 = Mid-Height
3 = Full-Height

D = FPGA

1 = EP2SGX90
2 = EP2SGX130

E = FPGA SPEED

1 = Low
2 = High

F = ADC

1 = 130 MSPS @ 16-bit
2 = 200 MSPS @ 16-bit

J = Conformal Coating

0 = None
1 = Humiseal 1A33 Polyurethane
2 = Humiseal 1B31 Acrylic

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