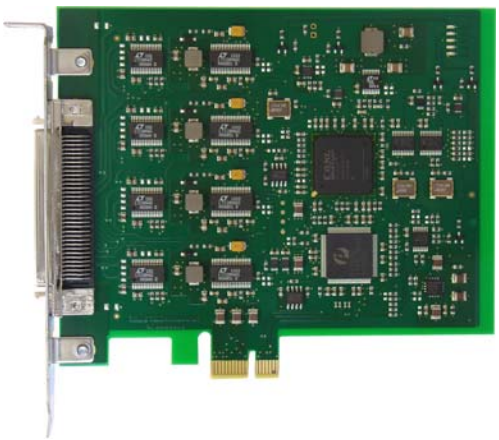
TPCE863 4 Channel High Speed Synch/Asynch Serial Interface

Application Information

The TPCE863 is a standard height, half length PCI Express 1.1 compliant module with four high speed serial data communication channels.

The serial communication controller is implemented in FPGA logic, along with a bus master capable PCI interface, guaranteeing long term availability with the option to implement additional functions in the future. The FPGA is connected to the PCI Express interface via a transparent PCI Express to PCI bridge.



Each channel has a receive and a transmit FIFO of 512 long words (32 bit) per channel for high data throughput.

Data transfer on the PCI Express bus is handled via TPCE863 initiated DMA cycles with minimum host/CPU intervention.

Several serial communication protocols are supported by each channel, such as asynchronous, isochronous, synchronous and HDLC mode.

A 14.7456 MHz oscillator provides standard asynchronous baud rates. A 24 MHz and a 10 MHz oscillator are provided for other (synchronous) baud rates.

Additionally each channel provides various interrupt sources, generated on INTA. The interrupt sources can be enabled or disabled individually.

Multiprotocol transceivers are used for the line interface. The physical interface is selectable by software, individually for each channel as EIA-232, EIA-422, EIA-449, EIA-530, EIA-530A, V.35, V.36 or X.21.

A HD68 SCSI-3 type connector at the front panel provides access to the I/O lines.

The following signals are provided by the TPCE863 for each channel at the front I/O connector:

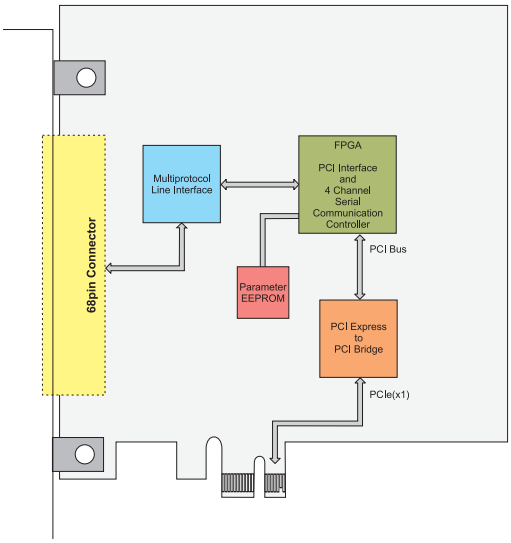
Receive Data (RxD +/-), Transmit Data (TxD +/-), Receive Clock (RxC +/-), Transmit Clock (TxC +/-), Ready-To-Send (RTS +/-), Clear-To-Send (CTS +/-), Carrier-Detect (CD +/-) and GND. Additionally, serial channel 3 provides Data-Set-Ready (DSR3 +/-) and Data-Terminal-Ready (DTR3 +/-).

A serial EEPROM is used to store detailed board information and special configuration parameters.

For First-Time-Buyers the engineering documentation TPCE863-ED is recommended. The engineering documentation includes TPCE863-DOC, schematics and data sheets of TPCE863 devices.

Technical Information

- Form Factor: PCISIG PCI Express Revision 1.1
  - Board size: 129.4 mm x 106.7 mm
  - Standard height, half length
- Four high speed synchronous/asynchronous serial interfaces
- Support of RxD, TxD, RxC, TxC, RTS, CTS, CD and GND on front connector, DTR3 and DSR3 on channel 3 only
- Physical interface (individually programmable per channel):
  EIA-232, EIA-422, EIA-449, EIA-530, EIA-530A, V.35, V.36 and X.21
- Maximum data rate: 10 Mbit/s (synchronous),
  2 Mbit/s (asynchronous), internal or external provided clock
- EIA-232: up to 115.2 kbit/s
- Temperature range: -40°C to +85°C



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Order Information

RoHS Compliant

TPCE863-10R	4 Channel High Speed Synch/Asynch Serial Interface

Documentation

TPCE863-DOC	User Manual
TPCE863-ED	Engineering documentation (TPCE863-DOC, Schematics, Assembly Drawing, Data Sheets)

Software

TDRV009-SW-25	Integrity Software Support
TDRV009-SW-42	VxWorks Software Support (Legacy and VxBus-Enabled Software Support)
TDRV009-SW-65	Windows XP/XPE/2000 Software Support
TDRV009-SW-72	LynxOS Software Support
TDRV009-SW-82	Linux Software Support
TDRV009-SW-95	QNX 6 Software Support

For other operating systems please contact TEWS.

Related Products

TA304	Cable Kit for modules with HD68 connector

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