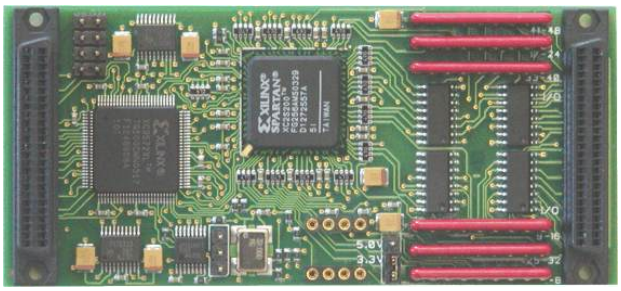
TIP630 Reconfigurable FPGA with 48 TTL I/O

Application Information

The TIP630 is an IndustryPack® compatible module providing a user configurable FPGA with 200,000 system gates. 48 I/O lines of the FPGA are directly connected to the IP I/O connector. Each I/O line has a series damping resistor and is protected against ESD and overvoltage. Six pull up resistor networks mounted in sockets are provided for the I/O lines. Pull up voltage is selectable to be either +3.3V or +5V. The I/O lines are individually programmable as input, output or tri-state I/O.

All IP bus signals of the IP interface are routed to the FPGA allowing to implement 8 MHz or 32 MHz bus interfaces with or without DMA.

Several clock sources are available at the FPGA: the IP clock (8 MHz or 32 MHz), a local 32 MHz clock and two outputs of the programmable clock generator (250 KHz – 166 MHz).



The FPGA can be configured via the IP bus or optional by a PROM which can be mounted in a socket. The configuration download for the FPGA and the programming of the clock generator is implemented by a CPLD reserving the upper two 16 bit registers of the IP I/O space. After the FPGA has been configured with the user application it can be accessed via the IP bus. The CPLD can be used for reprogramming the FPGA without turning power off. Furthermore the CPLD offers a default ID-Prom contents which can stay active after configuring the FPGA or it can be switched off and replaced by a user ID-PROM implemented in the FPGA.

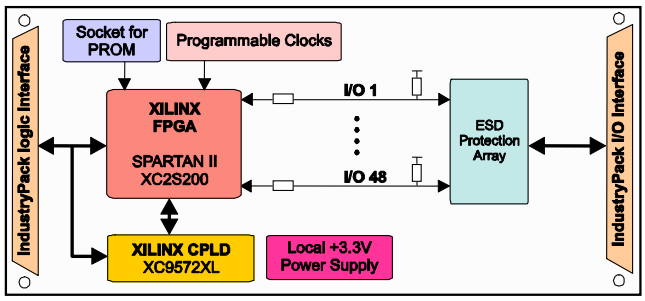
User applications can be developed using the design software ISE WebPACK which can be downloaded free of charge from www.xilinx.com .

For First Time Users the Engineering Documentation TIP630-ED is recommended. The Engineering Documentation includes TIP630-DOC, schematics, data sheets / application notes of the components and well documented sample VHDL source code.

Software support (TIP630-SW-xx) is available for different operating systems.

Technical Information

- Interface according to IndustryPack specification
- Single Size IndustryPack
- Xilinx XC2S200-5 SpartanII FPGA logic configurable via IP bus or optional by PROM XC17S200APD8I
- All IP bus interface signals routed to the FPGA
- FPGA clock options:
  - IP bus clock (8 or 32 MHz)
  - Local 32 MHz clock oscillator
  - PLL programmable clock generator CY22150 (250 KHz – 166 MHz), 2 clock outputs connected to FPGA
- 48 digital TTL I/O lines
  - I/O lines individually programmable as input, output, tri-state I/O
  - 6 pull up resistor networks mounted in sockets
  - jumper selectable +3.3V or +5V common for all pull up resistor networks
  - ESD and overvoltage protection for each I/O line
- Operating temperature range -40°C to +85°C



TEWS TECHNOLOGIES GmbH
Am Bahnhof 7 25469 Halstenbek, Germany
Phone: +49 (0) 4101 4058 0 Fax: +49 (0) 4101 4058 19
e-mail: info@tews.com www.tews.com

Order Information

RoHS Compliant

TIP630-10R	Reconfigurable FPGA logic with 48 TTL I/O lines

None RoHS Compliant

TIP630-10	None RoHS compliant version of TIP630-10R

Documentation

TIP630-DOC	User Manual
TIP630-ED	Engineering Documentation, includes TIP630-DOC

Software

TIP630-SW-25	Integrity Software Support
TIP630-SW-42	VxWorks Software Support (Legacy and VxBus-Enabled Software Support)
TIP630-SW-65	Windows XP/XPE/2000 Software Support
TIP630-SW-72	LynxOS Software Support
TIP630-SW-82	LiNUX Software Support
TIP630-SW-95	QNX 6 Software Support

For other operating systems please contact TEWS.

TEWS TECHNOLOGIES GmbH
Am Bahnhof 7 25469 Halstenbek, Germany
Phone: +49 (0) 4101 4058 0 Fax: +49 (0) 4101 4058 19
e-mail: info@tews.com www.tews.com