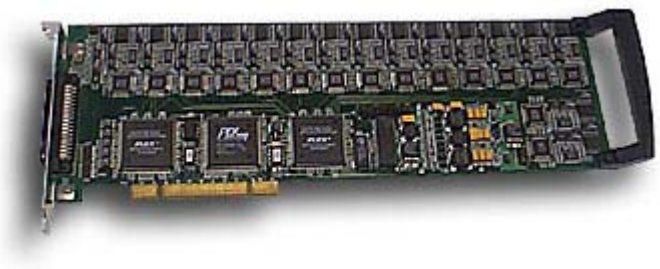
General Standards Corporation

High Performance Bus Interface Solutions

PCI-16SDI

16-Channel, 16-Bit Sigma-Delta Analog Input PCI Board

With 220 KSPS Sample Rate per Channel, and 4 Independent Clocks



Features Include:

- Sigma-Delta Conversion; No External Antialiasing Filters Required
- High Effective Sampling Rate
- Integral Antialiasing Input Filters Reject Out-of-Band Interference Components
- Completely Software Configurable; No Field Configuration Jumpers
- Sixteen 16-Bit Analog Input Channels; Dedicated Sigma-Delta Converter per Channel
- Sample Rates Selectable from 5K to 220K Samples per Second per Channel
- Four Independent Sample-Rate Generators; Adjustable with 0.2 Percent Resolution
- 256K-Sample FIFO Buffer. All Data is Channel-Tagged
- Two-Channel DMA Engine Supports Block and Demand-Mode Transfers
- Harmonic Sampling Supported, with Interchannel Clocking Ratios from 1 to 32
- Auto calibration Uses Hardware Correction; No missing Codes Introduced
- Optional 68-Pin 2-Row or 50-Pin D-Subminiature System I/O Connector
- Windows NT™ & Solaris™ drivers available
- Universal 3.3V, 5V PCI Signaling
- Standard PCI Form Factor

Applications Include:

- ✓ Acoustics Analysis
- ✓ Analog Inputs
- ✓ Data Acquisition Systems
- ✓ Voltage Measurement
- ✓ Process Monitoring
- ✓ Industrial Robotics
- ✓ Automatic Test Equipment
- ✓ Audio Waveform Analysis
- ✓ Environmental Test Systems

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Overview:

The 16-channel PCI-16SDI analog input board provides high-density precision 16-bit analog input resources on a standard PCI expansion board. Optimized for flexibility and performance, the board is ideal for a wide variety of applications, ranging from simple precision voltage measurements, to the analysis of complex audio signals and waveforms. Each of the 16 sigma-delta analog input channels can be controlled by any one of four independent sample clocks, and multiple channels can be harmonically locked together. A/D conversions on multiple boards can be synchronized and phase-locked. Sample rates are adjustable from 5 KSPS to 220 KSPS, and the input range is software selectable as ±1.25V, ±2.5V, ±5V or ±10V. Internal autocalibration networks permit periodic calibration to be performed without removing the board from the system.

Each ADC contains a digital antialiasing filter that rejects out-of-band signals above approximately 48 percent of the selected sample rate. Lowpass analog input filters remove those interference signals that fall within the harmonic images of the digital filter, the first of which occurs at 64 times the sample rate. Four independent sample-rate clock generators are individually adjustable from 8 MHz to 16 MHz, and are divided down within the local controller to provide individual channel sample rates from 5 KSPS to 220 KSPS. Conversion data from all active channels is transferred to the PCI bus through a 256K-sample data buffer that provides a software controlled threshold for generating interrupt requests.

Multiple channels can be synchronized to perform sampling in "lockstep", either by a software command, or by external hardware sync and clock input signals. Hardware sync and clock input/output signals permit multiple boards to be daisy-chained together for phase-locked operation from a common clock.

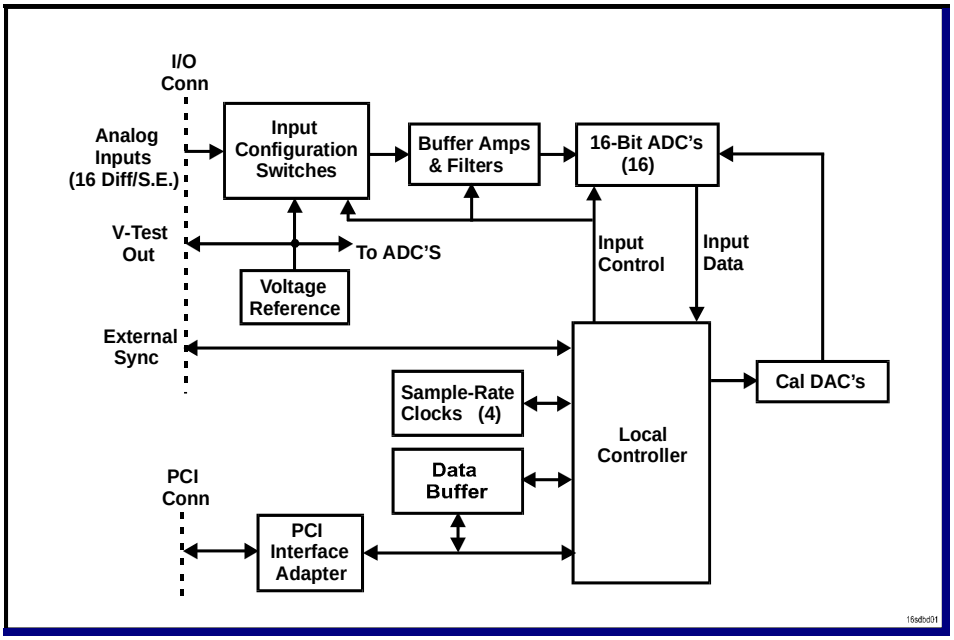

Figure 1. PCI-16SDI; Functional Organization

The board is functionally compatible with the IEEE PCI local bus specification Revision 2.3, and supports the "plug-n-play" initialization concept. System input/output connections are made at the panel bracket through a single 68-pin, 0.05" dual-ribbon I/O connector, or through an optional 50-Pin D-subminiature connector. Power requirements consist of +5 VDC, in compliance with the PCI specification, and operation over the specified temperature range is achieved with minimal (200 LFPM) air cooling.

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ELECTRICAL SPECIFICATIONS

At +25 ^{O}C, with specified operating conditions.

Input Channel Characteristics:

Configuration:	16 input channels, software controlled as differential or single-ended. Optional 4 and 8-channel configurations available.
Voltage Range:	Software Configurable as ±1.25 Volts, ±2.5 Volts, ±5 Volts or ±10 Volts
Input Impedance:	1.0 Megohm typical, in parallel with 20 pF. 2 Megohms line-line.
Common Mode Rejection:	80 dB minimum, DC-60 Hz (Differential mode)
Common Mode Range:	±11 Volts with zero normal-mode input
Offset Voltage:	±0.6 millivolts, maximum
Noise:	1.5LSB-RMS on all ranges, 10Hz-100KHz, typical.
Overvoltage Protection:	±30-Volt transients with power applied; ±15 Volts with power removed

Transfer Characteristics:

Resolution:	16 Bits (0.0015 percent of FSR)
Sample Rate:	5,000 to 220,000 samples per second per channel
Oversampling Factor:	x64

DC Accuracy:
(Maximum composite error)

Range	Midscale Accuracy	±Fullscale Accuracy
±10V	±1.2mv	±5.2mv
±5V	±1.1mv	±3.1mv
±2.5V	±0.9mv	±2.2mv
±1.25V	±0.8mv	±1.5mv

Bandwidth:	DC to approximately 48 percent of the selected sample rate
Crosstalk Rejection:	80 dB typical, DC-2 kHz
Antialias Filtering:	Each ADC provides internal antialias filtering at 48 percent of the selected sample rate. This digital filter is supported by a multi-pole analog antialiasing input filter with a cutoff frequency that is determined by the selected sample rate and the oversampling factor (x64).
Integral Nonlinearity:	±0.003 percent of FSR, typical
Differential Nonlinearity:	±0.0015 percent of FSR, maximum
Total Harmonic Distortion:	84 dB typical, from DC to 40 percent of sample rate

Operating Modes and Controls:

Organization:	Four 4-channel analog input groups, and four sample rate generators. Each channel group can operate from any rate generator. The sample rate for each individual channel is selected by dividing the frequency of the assigned rate generator by any integer from 1 through 32.
Sample Rate Generators:	Four independent internal rate generators, each adjustable from 16-32 MHz, are divided by 128 to provide four independent sample rate sources. Subsequent division by an integer from 1 to 32 for each channel provides sample rates from 3.9 KSPS to 250 KSPS. (Specified performance is guaranteed within the range from 5 KSPS to 220 KSPS). Setting resolution is 0.2 percent or less, and setting accuracy is ±0.015 percent. *

* Accuracy is 0.08 percent on earlier boards. Contact factory for details.

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Operating Modes and Controls (Continued):

External Clock I/O:	An LVDS hardware output clock can be derived either from a 16-32 MHz LVDS external hardware input clock, or from an internal rate generator. The external clock input can be selected as the rate generator for any or all channels. Multiple boards can be locked to a common clock by daisy-chaining the output clock from each board to the input clock of the next board in the chain. This requires a split I/O cable. As many as eight boards can be daisy-chained together.
Synchronization:	Sampling can be synchronized within each channel group through software, or each group can be synchronized to an external LVDS hardware sync input. By using the daisy-chain configuration described for External Clock I/O, hardware sync inputs and outputs can be used to synchronize sampling among multiple boards.
Harmonic Sampling:	Harmonic sampling ratios are implemented by adjusting the sample rates of channels within a group to specific fractions of the assigned rate generator frequency. (See Sample Rate Generators).
Data Format:	Software selected as either offset binary or two's complement
Channel Tags:	Each input data value is appended with a 4-bit channel identification tag.
Buffer Threshold Flags:	A threshold flag is asserted when the number of samples in the selected buffer exceeds the selected threshold. The buffer threshold can be any integer from 0 0000 to 3 FFFEh.

PCI Compatibility:

Conforms to PCI Specification 2.3: D32, 33MHz, 3.3V/5V signaling.
Supports "plug-n-play" initialization.
Single multifunction interrupt.
2-Channel DMA in block and demand modes.

Board Control and Data Registers:

Board Control/Status Register:	Determines the principal operating mode.
Rate Generator Registers:	Select rate generator frequencies.
Channel Control Registers:	Control the clock sources and sample rates for all input channels.
Input Data Buffer:	256K by 20-Bit FIFO buffer.
Buffer Threshold:	Selects the input data buffer threshold.
Interrupt Control:	Interrupt source control and status.

Analog Input Buffer

Analog input data is read through a 256K-sample FIFO buffer as a 20-Bit data field for each input sample. The data field contains a 16-Bit conversion value and a 4-Bit channel tag. A threshold flag occurs when the associated buffer contains a number of data samples that exceeds a software-selected threshold from 0 0000h to 3 FFFEh, and can be used to generate empty and full flags.

MECHANICAL AND ENVIRONMENTAL SPECIFICATIONS

Power Requirements

+5.0 VDC ±0.20 VDC at 4.5 Amps, maximum

Physical Dimensions (Excluding panel bracket)

Height: 106.7 mm (4.20 in)
Depth: 312.0 mm (12.28 00 in)
Width: 21.6 mm (0.85 in)

Environmental Specifications

Ambient Temperature Range:	Operating: 0 to +65 degrees Celsius inlet air Storage: -40 to +85 degrees Celsius
Relative Humidity:	Operating: 0 to 80%, non-condensing Storage: 0 to 95%, non-condensing
Altitude:	Operation to 10,000 ft.

Cooling Requirements

200 LFPM minimum air flow across component side of board; .

ORDERING INFORMATION

Specify the basic product model number (PCI-16SDI), followed by an option suffix "-A-B", as indicated below. For example, model number PCI-16SDI-16-DB50 describes a board with 16 input channels and a 50-Pin D-subminiature system I/O connector.

Optional Parameter	Value	Specify Option As:
Number of Input Channels:	4 Channels	A = 4
	8 Channels	A = 8
	16 Channels	A = 16
System I/O Connector:	68-Pin 2-Row	B = RN68
	50-Pin D-Subminiature	B = DB50

SYSTEM I/O CONNECTIONS

Table 1. 68-Pin System Connector Pin Functions

P2, ROW-A (Cable-A)		P2, ROW-B (Cable-B)	
PIN	SIGNAL	PIN	SIGNAL
1	DIGITAL RETURN	1	DIGITAL RETURN
2	DIGITAL RETURN	2	DIGITAL RETURN
3	CLOCK INPUT LO	3	CLOCK OUTPUT LO
4	CLOCK INPUT HI	4	CLOCK OUTPUT HI
5	DIGITAL RETURN	5	DIGITAL RETURN
6	DIGITAL RETURN	6	DIGITAL RETURN
7	SYNC INPUT LO	7	SYNC OUTPUT LO
8	SYNC INPUT HI	8	SYNC OUTPUT HI
9	DIGITAL RETURN	9	DIGITAL RETURN
10	DIGITAL RETURN	10	DIGITAL RETURN
11	INPUT RETURN	11	INPUT RETURN
12	INPUT RETURN	12	INPUT RETURN
13	INPUT RETURN	13	INPUT RETURN
14	INPUT RETURN	14	INPUT RETURN
15	VTEST RETURN	15	INPUT RETURN
16	VTEST OUTPUT	16	INPUT RETURN
17	INPUT CHAN 07 LO	17	INPUT CHAN 15 LO
18	INPUT CHAN 07 HI	18	INPUT CHAN 15 HI
19	INPUT CHAN 06 LO	19	INPUT CHAN 14 LO
20	INPUT CHAN 06 HI	20	INPUT CHAN 14 HI
21	INPUT CHAN 05 LO	21	INPUT CHAN 13 LO
22	INPUT CHAN 05 HI	22	INPUT CHAN 13 HI
23	INPUT CHAN 04 LO	23	INPUT CHAN 12 LO
24	INPUT CHAN 04 HI	24	INPUT CHAN 12 HI
25	INPUT CHAN 03 LO	25	INPUT CHAN 11 LO
26	INPUT CHAN 03 HI	26	INPUT CHAN 11 HI
27	INPUT CHAN 02 LO	27	INPUT CHAN 10 LO
28	INPUT CHAN 02 HI	28	INPUT CHAN 10 HI
29	INPUT CHAN 01 LO	29	INPUT CHAN 09 LO
30	INPUT CHAN 01 HI	30	INPUT CHAN 09 HI
31	INPUT CHAN 00 LO	31	INPUT CHAN 08 LO
32	INPUT CHAN 00 HI	32	INPUT CHAN 08 HI
33	INPUT RETURN	33	INPUT RETURN
34	INPUT RETURN	34	INPUT RETURN

(See reference manual for optional 50-Pin D-subminiature connector pinout)

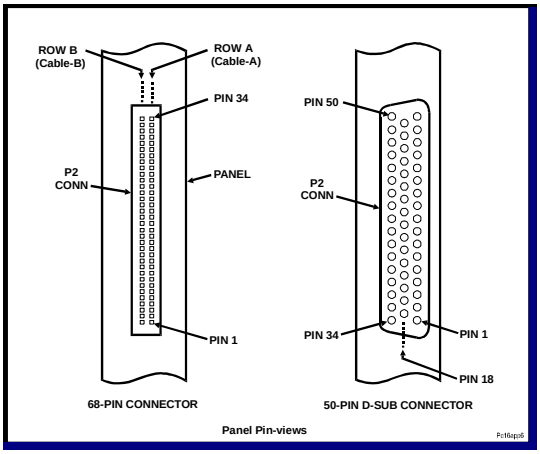

Figure 2. System I/O Connector

System Mating Connector:

68-Pin 2-row 0.050" dual ribbon-cable socket connector:
Robinson Nugent # P50E-068-S-TG;

Or,

50-Pin D-subminiature IDC connector:
AMP # 746790-1, with strain-relief:
AMP # 746785-1.

Contact factory for availability of the 68-pin AMP SCSI-3 connector.