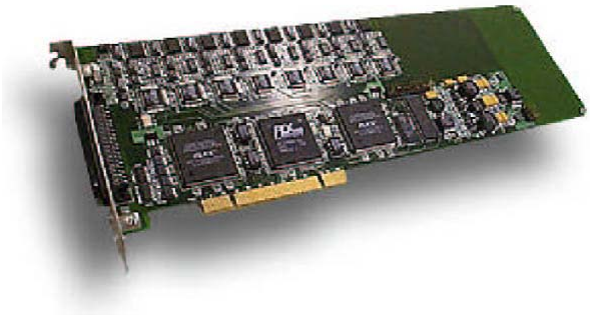
General Standards Corporation

High Performance Bus Interface Solutions

PCI-16HSDI

8-Channel, 16-Bit Sigma-Delta Analog Input PCI Board

With 1.1 MSPS Sample Rate per Channel, and High-Rate Buffer



Features Include:

- Sigma-Delta Conversion; No External Antialiasing Filters Required
- High Effective Sampling Rate
- Integral Antialiasing Input Filters Reject Out-of-Band Interference Components
- Completely Software Configurable; No Field Configuration Jumpers
- Eight 16-Bit Analog Input Channels; Dedicated Sigma-Delta Converter per Channel
- Sample Rates Selectable from 30K to 1100K Samples per Second per Channel
- Four Independent Sample-Rate Generators; Adjustable with 0.2 Percent Resolution
- 256K-Sample High-Rate FIFO Buffer. All Data is Channel-Tagged
- 2-Channel DMA engine; Block and Demand-Mode Transfers
- Harmonic Sampling Supported, with Interchannel Clocking Ratios from 1 to 32
- Auto calibration Uses Hardware Correction; No missing Codes Introduced
- Input Ranges Selectable as ±1.25V, ±2.5V, ±5V or ±10V
- Optional 4-Channel version available
- Universal 3.3V, 5V Signaling
- Standard PCI Form Factor

Applications Include:

- ✓ Acoustics Analysis
- ✓ Analog Inputs
- ✓ Data Acquisition Systems
- ✓ Voltage Measurement
- ✓ Process Monitoring
- ✓ Industrial Robotics
- ✓ Automatic Test Equipment
- ✓ Audio Waveform Analysis
- ✓ Environmental Test Systems

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Overview:

The 8-channel PCI-16HSDI analog input board provides high-density precision 16-bit analog input resources on a standard PCI expansion board. Optimized for flexibility and performance, the board is ideal for a wide variety of applications, ranging from simple precision voltage measurements, to the analysis of complex audio signals and waveforms. Each of the eight sigma-delta analog input channels can be controlled by any one of four independent sample clocks, and multiple channels can be harmonically locked together. A/D conversions on multiple boards can be synchronized and phase-locked. Sample rates are adjustable from 30 KSPS to 1.1 MSPS, and the input range is software selectable as ±1.25V, ±2.5V, ±5V or ±10V. Internal autocalibration networks permit periodic calibration to be performed without removing the board from the system.

Each ADC contains a digital antialiasing filter that rejects out-of-band signals above approximately 48 percent of the selected sample rate. Lowpass analog input filters remove those interference signals that fall within the harmonic images of the digital filter, the first of which occurs at 16-32 times the sample rate.

Multiple channels can be synchronized to perform sampling in "lockstep", either by a software command, or by external hardware sync and clock input signals. Hardware sync and clock input/output signals permit multiple boards to be daisy-chained together for phase-locked operation from a common clock.

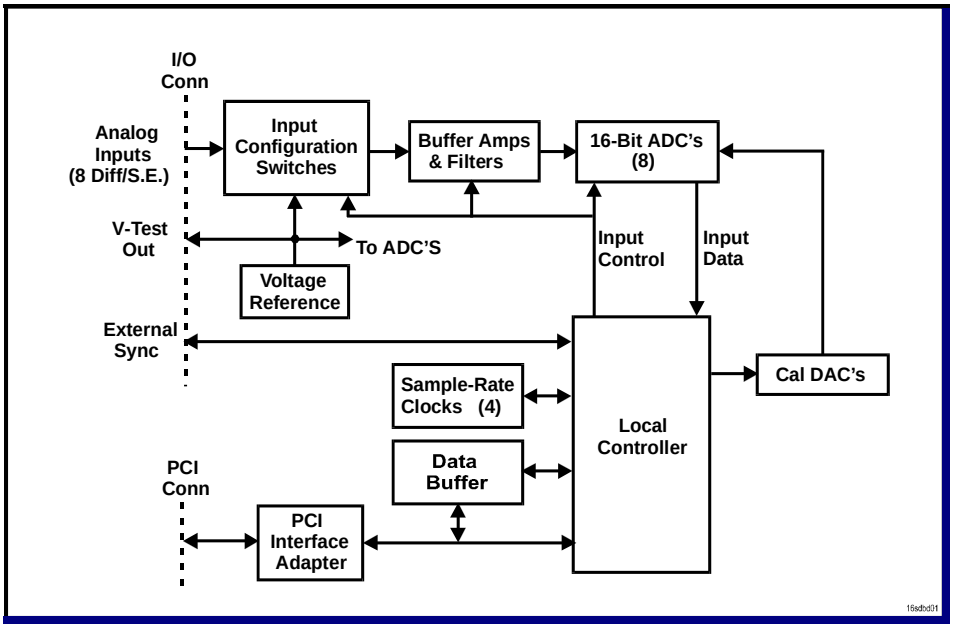

Figure 1. PCI-16HSDI; Functional Organization

This product is functionally compatible with the IEEE PCI local bus specification Revision 2.3 , and supports the "plug-n-play" initialization concept. System input/output connections are made through a single 68-pin, 0.05" dual ribbon connector or optional 50-Pin D-Subminiature connector. Power requirements consist of +5 VDC, in compliance with the PCI specification, and operation over the specified temperature range is achieved with minimal air cooling.

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ELECTRICAL SPECIFICATIONS

At +25 ^{O}C, with specified operating voltages.

Input Channel Characteristics:

Configuration:	8 input channels, software controlled as differential or single-ended. Optional 4-channel configuration available.
Voltage Range:	Software Configurable as ±1.25 Volts, ±2.5 Volts, ±5 Volts or ±10 Volts
Input Impedance:	1.0 Megohm typical, in parallel with 20 pF. 2 Megohms line-line.
Common Mode Rejection:	80 dB minimum, DC-60 Hz (Differential mode)
Common Mode Range:	±11 Volts with zero normal-mode input
Offset Voltage:	±0.6 millivolts, maximum
Noise:	3.0LSB-RMS on all ranges, 10Hz-500KHz, typical.
Overvoltage Protection:	±30-Volt transients with power applied; ±15 Volts with power removed

Transfer Characteristics:

Resolution:	16 Bits (0.0015 percent of FSR)
Sample Rate:	30 KSPS to 1100 KSPS (thousand samples per second) per channel
Oversampling Factor:	x32 for sample rates from 30 KSPS to 600 KSPS, x16 above 600 KSPS.

DC Accuracy: (Maximum composite error)

Range	Midscale Accuracy	±Fullscale Accuracy
±10V	±1.2mv	±5.2mv
±5V	±1.1mv	±3.1mv
±2.5V	±0.9mv	±2.2mv
±1.25V	±0.8mv	±1.5mv

Small Signal Bandwidth:	DC to approximately 48 percent of the selected sample rate
Power Bandwidth:	DC to 5*10^{6} Hz-Vpp minimum. Accepts 500kHz input at 10 VPP.
Crosstalk Rejection:	80 dB typical, DC-10 kHz
Antialias Filtering:	Each ADC provides internal antialias filtering at 48 percent of the selected sample rate. This digital filter is supported by a multi-pole analog antialiasing input filter with a cutoff frequency that is determined by the selected sample rate and the oversampling factor (x64).
Integral Nonlinearity:	±0.003 percent of FSR, typical
Differential Nonlinearity:	±0.0015 percent of FSR, maximum
Total Harmonic Distortion:	83 dB typical, from DC to 40 percent of sample rate

Operating Modes and Controls:

Organization:	Four 4-channel analog input groups, and four sample rate generators. Each channel group can operate from any rate generator. The sample rate for each individual channel is selected by dividing the frequency of the assigned rate generator by any integer from 1 through 20.

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Operating Modes and Controls (Continued):

Sample Rate Generators:	Each of four independent internal rate generators can be assigned to any input channel group. Each generator is adjustable from 19.2 MHz to 38.4 MHz, and provides sample rates from 600 KSPS to 1200 KSPS after division by 32 (x16 oversampling), or from 300 KSPS to 600 KSPS after division by 64 (x32 oversampling). Subsequent division by an integer from 1 to 20 for each channel provides sample rates from 15 KSPS to 1200 KSPS. (Specified performance is guaranteed within the range from 30 KSPS to 1100 KSPS). Settling time when changing frequencies is approximately 20 ms, and settling completion is selectable as an interrupt event. Setting resolution is 0.2 percent or less; accuracy is ±0.015 percent.
External Clock I/O:	A hardware output clock can be derived either from an external LVDS hardware input clock or from an internal rate generator. The external clock input can be selected as the conversion clock for any or all channels. I/O clocks are LVDS signals, and have a frequency range of 19.2 MHz to 38.4 MHz. Multiple boards can be locked to a common clock by daisy-chaining the output clock from each board to the input clock of the next board in the chain. As many as six boards can be daisy-chained together.
Synchronization:	Sampling can be synchronized within each channel group through software, or each group can be synchronized to an external LVDS hardware sync input. By using the daisy-chain configuration described for External Clock I/O, hardware sync inputs and outputs can be used to synchronize the sampling among multiple boards.
Harmonic Sampling:	Harmonic sampling ratios are implemented by adjusting the sample rates of channels within a group to specific fractions of the assigned rate generator frequency. (See Sample Rate Generators).
Data Format:	Software selected as either offset binary or two's complement
Channel Tags:	Each input data value is appended with a 3-bit channel identification tag.
Buffer Threshold Flags:	A threshold flag is asserted when the number of samples in the selected buffer exceeds the selected threshold. The buffer threshold can be any integer from 0 0000 to 3 FFFEh.

PCI Compatibility:

Conforms to PCI Specification 2.3: D32, 33MHz, 3.3V/5V signaling,
Supports "plug-n-play" initialization,
Multifunction interrupt,
DMA in two channels as bus master; block and demand-mode transfers

Analog Input Buffer:

Analog input data is read through a 256K-sample FIFO buffer as a 20-Bit data field for each input sample. The data field contains a 16-Bit conversion value and a 3-Bit channel tag. A threshold flag occurs when the associated buffer contains a number of data samples that exceeds a software-selected threshold from 0 0000h to 3 FFFEh, and can be used to generate empty and full flags.

To increase the transfer rate of data from the local bus to the PCI adapter, the original emulated FIFO that was implemented in the PCI-16SDIHS product series has been replaced with a true FIFO.

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MECHANICAL AND ENVIRONMENTAL SPECIFICATIONS

Power Requirements:

+5.0 VDC ±0.20 VDC at 3.5 Amps, maximum; 2.7 Amps typical.

Physical Dimensions (Excluding panel bracket):

Height: 106.7 mm (4.20 in)
Depth: 312.0 mm (12.28 00 in)
Width: 21.6 mm (0.85 in)

Environmental Specifications:

Ambient Temperature Range:	Operating: 0 to +65 degrees Celsius inlet air Storage: -40 to +85 degrees Celsius
Relative Humidity:	Operating: 0 to 80%, non-condensing Storage: 0 to 95%, non-condensing
Altitude:	Operation to 10,000 ft.

Cooling Requirements:

100 LFPM minimum air flow across component side of board; .

ORDERING INFORMATION

Specify the basic product model number (PCI-16HSDI), followed by an option suffix "-A-B", as indicated below. For example, model number PCI-16HSDI-8-DB50 describes a board with eight input channels and a 50-Pin D-Subminiature system I/O connector.

Optional Parameter	Value	Specify Option As:
Number of Input Channels:	4 Channels	A = 4
	8 Channels	A = 8
I/O Connector Type:	DB50 D-Submin	B = DB50
	68-Pin IDC	B = RN68

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SYSTEM I/O CONNECTIONS

Table 1. System Connector Pin Functions

68-PIN I/O CONNECTOR				
ROW-A (Cable-A)			ROW-B (Cable-B)	
PIN	SIGNAL		PIN	SIGNAL
1	DIGITAL RETURN		1	DIGITAL RETURN
2	DIGITAL RETURN		2	DIGITAL RETURN
3	CLOCK INPUT LO		3	CLOCK OUTPUT LO
4	CLOCK INPUT HI		4	CLOCK OUTPUT HI
5	DIGITAL RETURN		5	DIGITAL RETURN
6	DIGITAL RETURN		6	DIGITAL RETURN
7	SYNC INPUT LO		7	SYNC OUTPUT LO
8	SYNC INPUT HI		8	SYNC OUTPUT HI
9	DIGITAL RETURN		9	DIGITAL RETURN
10	DIGITAL RETURN		10	DIGITAL RETURN
11	INPUT RETURN		11	INPUT RETURN
12	INPUT RETURN		12	INPUT RETURN
13	INPUT RETURN		13	INPUT RETURN
14	INPUT RETURN		14	INPUT RETURN
15	VTEST RETURN		15	INPUT RETURN
16	VTEST OUTPUT		16	INPUT RETURN
17	INPUT CHAN 07 LO		17	INPUT RETURN
18	INPUT CHAN 07 HI		18	INPUT RETURN
19	INPUT CHAN 06 LO		19	INPUT RETURN
20	INPUT CHAN 06 HI		20	INPUT RETURN
21	INPUT CHAN 05 LO		21	INPUT RETURN
22	INPUT CHAN 05 HI		22	INPUT RETURN
23	INPUT CHAN 04 LO		23	INPUT RETURN
24	INPUT CHAN 04 HI		24	INPUT RETURN
25	INPUT CHAN 03 LO		25	INPUT RETURN
26	INPUT CHAN 03 HI		26	INPUT RETURN
27	INPUT CHAN 02 LO		27	INPUT RETURN
28	INPUT CHAN 02 HI		28	INPUT RETURN
29	INPUT CHAN 01 LO		29	INPUT RETURN
30	INPUT CHAN 01 HI		30	INPUT RETURN
31	INPUT CHAN 00 LO		31	INPUT RETURN
32	INPUT CHAN 00 HI		32	INPUT RETURN
33	INPUT RETURN		33	INPUT RETURN
34	INPUT RETURN		34	INPUT RETURN

50-PIN D-SUB I/O CONNECTOR				
PIN	SIGNAL		PIN	SIGNAL
1	CLOCK INPUT LO		42	INPUT RETURN
34	CLOCK INPUT HI		26	INPUT CH 05 LO
18	SYNC INPUT LO		10	INPUT CH 05 HI
2	SYNC INPUT HI		43	INPUT RETURN
35	DIGITAL RETURN		27	INPUT RETURN
19	DIGITAL RETURN		11	INPUT CH 04 LO
3	CLOCK OUTPUT LO		44	INPUT CH 04 HI
36	CLOCK OUTPUT HI		28	INPUT RETURN
20	SYNC OUTPUT LO		12	INPUT RETURN
4	SYNC OUTPUT HI		45	INPUT CH 03 LO
37	INPUT RETURN		29	INPUT CH 03 HI
21	INPUT RETURN		13	INPUT RETURN
5	VTEST RETURN		46	INPUT RETURN
38	VTEST OUTPUT		30	INPUT CH 02 LO
22	INPUT RETURN		14	INPUT CH 02 HI
6	INPUT RETURN		47	INPUT RETURN
39	INPUT RETURN		31	INPUT RETURN
23	INPUT RETURN		15	INPUT CH 01 LO
7	INPUT CH 07 LO		48	INPUT CH 01 HI
40	INPUT CH 07 HI		32	INPUT RETURN
24	INPUT RETURN		16	INPUT RETURN
8	INPUT RETURN		49	INPUT CH 00 LO
41	INPUT CH 06 LO		33	INPUT CH 00 HI
25	INPUT CH 06 HI		17	INPUT RETURN
9	INPUT RETURN		50	INPUT RETURN

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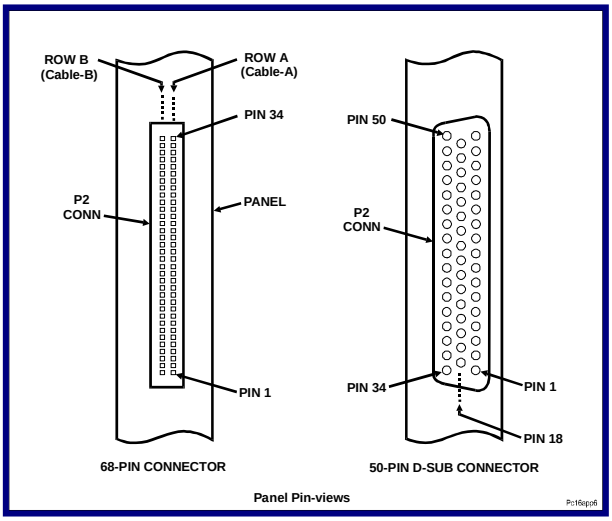

Figure 2. System Input/Output Connector

System Mating Connector:

68-Pin 2-row 0.050" dual ribbon-cable socket connector:
Robinson Nugent # P50E-068-S-TG;
or,

50-Pin D-subminiature IDC connector:
AMP # 746790-1, with strain-relief:
AMP # 746785-1.

Contact factory for availability of the 68-pin AMP SCSI-3 connector.

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