PCI-DMI32
Very High-speed Parallel Digital I/O Board
Up to 200 Mbytes/s Cable I/O
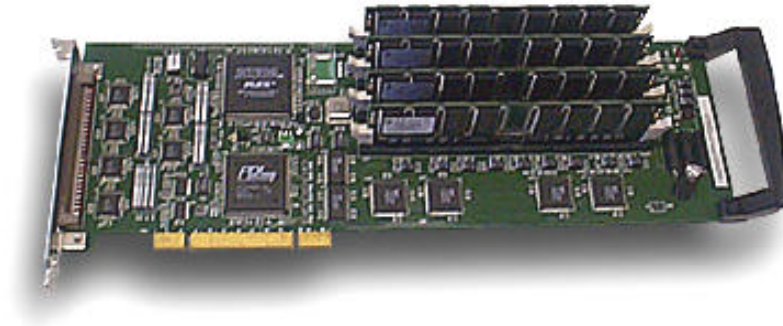
Features Include:

- The DMI will transfer up to 4GB of unique data continuously at up to 50 Mhz
- Provides for data I/O via the cable at up to 200 Mbytes per second (LVDS differential I/O)
- Can transfer data indefinitely without host intervention
- Bi-directional handshake signals can be user defined
- Windows NT driver available
- Buffers may be transmitted or received indefinitely without host intervention

Applications Include:

- ✓ High speed data acquisition and control
- ✓ Point-to-Point PMC-to-PMC bus communication
- ✓ High-speed video data capture
- ✓ General Purpose Parallel DMA interface
- ✓ Development and research
- ✓ Trainers and simulators

Functional Description:

The PCI-DMI32 Board provides a large on-board memory storage and high-speed, 32-bit parallel interface. It is capable of transmitting or receiving data transfers of up to 200 Mbytes per second on the cable.

The PCI-DMI32 Board includes up to 2GB of DRAM, a cable input/output controller, cable transceivers (differential, LVDS), and a DMA controller. The memory on the card is set to be either accessed from the PCI bus, or dedicated to the cable transfer. The on-board DRAM does not provide real-time access to the data from the PCI while a transfer is in progress. The DRAM is intended to be initialized over the PCI prior to the cable data transfer. When the transfer is enabled, the cable data will be either continuously transmitted from the on-board DRAM, or continuously received into the DRAM. Once the transfer is complete, the DRAM may be again accessed from the PCI bus.

The transfer controller is designed to allow several different transfer modes. In single transfer mode, a single buffer of data is transferred across the cable and then DRAM control is returned to the PCI bus. The single buffer may start at any address offset within the full 2GB DRAM space, and the transfer buffer size is also defined. In multi-buffer mode, multiple buffers may be transferred across the cable. In this manner, the user can define multiple buffers in the DRAM, which will then be transferred continuously to the cable when the transfer is enabled. On-board interrupts are defined to allow the user to update the start buffer address and buffer transfer size as soon as the transfer of one buffer begins. In this manner, the user can dynamically receive or transmit multiple buffers to/from the DRAM in one continuous transfer. Likewise, a single buffer can be transmitted continuously to the cable simply by not updating the start buffer address and buffer transfer size. This allows a continuous buffer of up to 2GB to be transmitted indefinitely on the cable.

Currently, the memory size of the PCI-DMI32 allows only 1GB or 2GB. Other memory sizes can be accommodated – consult factory for availability.

Note: The PCI-DMI32 is a long card and electrically compliant with PCI 2.1. Due to the height of the DRAM modules, the card requires three PCI slots.

Cable Interface:

The cable interface provides for very high-speed reception of data (up to 200 Mbytes/sec). The cable interface provides for a data interface width of 32 bits.
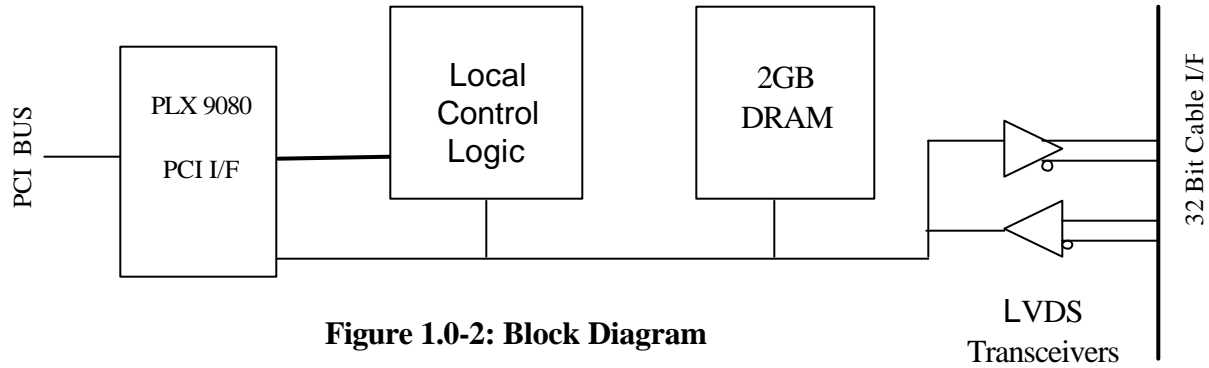

Figure 1.0-2: Block Diagram

High Performance Architecture:

The board is designed for the highest performance level using conventional (and moderately priced) components. The PCI-DMA engine is designed to require minimal intervention from the host; it provides for high-speed transfers between the FIFO and PCI memory using DMA instructions stored in RAM. Data is transferred from the cable to the FIFO using a high-speed dedicated I/O controller.

SPECIFICATIONS

DMA Transfer Rates

- Transfer Rate over cable (LVDS Transceivers):
  200 Mbytes/sec at 50 MHz clock rate and 32-bit cable interface.
- Transfer Rate over cable (Differential Pseudo ECL Transceivers):
  200 Mbytes/sec (max)
- PCI transfer rate from on-board Memory to PCI
- Data transfers over the cable do not interrupt data transfers over PCI since data is decoupled using memory buffering.

DMA Start Latency (when started by cable input or by CPU)

Initialization and DMA start: less than 1 microsecond typ.

Memory

The Memory on the PCI-DMI32 are used for buffering the transmit or receive data.

The board has the following Memory options:

Interrupts

Interrupt upon DMA engine done

Cable Interface Transceivers

LVDS

RS-422/485 transceivers provide +- 7.5 Volts of noise immunity and can withstand +- 25 Volt transients without damage.
Optional on-board parallel termination. The parallel terminators provide the usual transmission line termination. In either case unused inputs can be left open; however, the logic level of unconnected inputs is indeterminate.

PCI INTERFACE

❏ **Compatibility:**   Conforms to PCI Specification 2.1, with D32 read/write transactions.
Supports "plug-n-play" initialization.
Single multifunction interrupt.
Supports DMA transfers as bus master.

MECHANICAL AND ENVIRONMENTAL SPECIFICATIONS

❏ **Power Requirements**

+5.0 VDC ±0.20 VDC at 4.5 Amps, maximum

❏ **Physical Dimensions (Excluding panel bracket)**

Height: 106.7 mm (4.20 in)
Depth: 312.0 mm (12.28 00 in)
Width: 21.6 mm (0.85 in)

❏ **Environmental Specifications**

Ambient Temperature Range: Operating: 0 to +55 degrees Celsius
                                  Storage: -40 to +85 degrees Celsius

Relative Humidity: Operating: 0 to 80%, non-condensing
                                  Storage: 0 to 95%, non-condensing

Altitude: Operation to 10,000 ft.

❏ **Cooling Requirements**

200 LFPM minimum air flow across component side of board;

ORDERING INFORMATION

Specify the basic product model number (PCI-DMI32-XGB-LVDS), where "X" is an option code as indicated below. For example, model number PCI-DMI32-1GB-LVDS describes a board with a total of 1GByte of memory.

Other Examples Follow:

PCI-DMI32 with 2Gbyte of memory;
PCI-HPDI32-4GB-LVDS with 4Gbyte of memory;