

General Standards Corporation

High Performance Bus Interface Solutions

PC104P-24DSI12-4-16SDI

4-Channel Low-Power 24-Bit Delta-Sigma

PC104-Plus Analog Input Board

With 200 KSPS Sample Rate per Channel



FEATURES:

- ♦ **Four Differential 24-Bit Analog Input Channels**
- ♦ **Delta-Sigma Converter per Channel, with Linear Phase Digital Antialias Filtering**
- ♦ **Sample rates from 2 KSPS to 200 KSPS per Channel**
- ♦ **Low Power Consumption. 3.5 Watts Typical at 8KSPS.**
- ♦ **Software-Selectable Input Ranges: $\pm 2.5V$ or $\pm 5V$**
- ♦ **Software Compatibility with PC104P-16SDI**
- ♦ 256 K-sample FIFO Buffer
- ♦ Synchronous or Independent ADC Clocking
- ♦ Internal Sample Rate Generators
- ♦ Hardware Sync and Clock I/O for Multiboard Synchronization
- ♦ DMA Engine Supports both Block-Mode and Demand-Mode Transfers
- ♦ 100dB Dynamic Range to 100KSPS; 93 dB SINAD
- ♦ On-demand Autocalibration Ensures DC Precision as well as AC performance
- ♦ Integrated DC/DC Conversion and Regulation of Precision Internal Supply Voltages
- ♦ Conforms to PCI Bus Specification, Revision 2.3, with Universal Signaling

TYPICAL APPLICATIONS:

- | | | |
|-----------------|-----------------------|---------------------------|
| ✓ Sonar Arrays | ✓ Voltage Acquisition | ✓ Phase Comparison |
| ✓ Analog Inputs | ✓ Acoustic Research | ✓ Audio Waveform Analysis |

PRELIMINARY

REV 121406

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Overview:

The 4-channel PC104P-24DSI12-4-16SDI analog input board provides high-density 24-bit analog input resources on a standard PC104-Plus module. Optimized for flexibility and performance with minimum power consumption, the board is ideal for a wide variety of applications, ranging from basic voltage measurement to the analysis of complex audio signals and waveforms.

Functional Description:

Each of four analog input channels contains a lowpass image filter, and a delta-sigma A/D converter that provides digital antialias filtering. An internal voltage reference can be applied to all channels to support self-test operations and autocalibration. Gain and offset trimming is performed by applying correction values that are determined during on-demand autocalibration. A linear-phase digital antialiasing filter rejects out-of-band signals, and a lowpass analog filter reject those interference signals that fall within the harmonic images of the digital filter.

An internal adjustable sample-rate generator is divided down within the local controller to provide individual channel sample rates up to 200KSPS. Conversion data from all active channels is transferred to the PCI bus through a 256K-sample data buffer that is supported by two DMA channels. Multiple channels can be synchronized to perform sampling in "lockstep", either by a software command, or by external hardware sync and clock input signals.

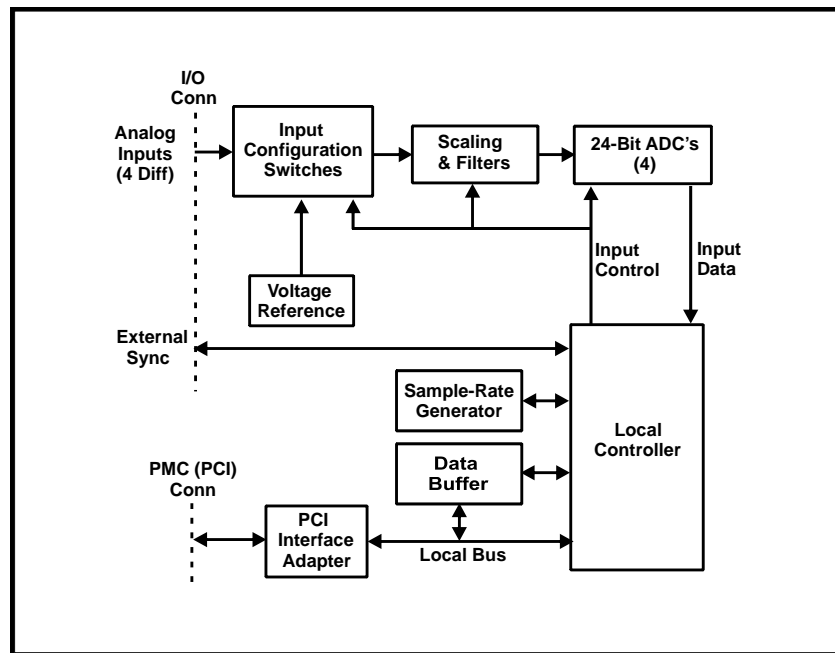


Figure 1. PC104P-24DSI12-4-16SDI; Functional Organization

This product is functionally compatible with the IEEE PCI local bus specification Revision 2.3. System input/output connections are made at the front panel through a high-density 68-Pin I/O connector. Power requirements consist of +5 VDC, in compliance with the PCI specification, and operation over the specified temperature range is achieved with conventional 100 LFPM air cooling.

ELECTRICAL SPECIFICATIONS

At +25 °C, with specified operating conditions.

Input Characteristics:

Configuration:	Four differential input channels.
Voltage Range:	Software Configurable as ± 2.5 Volts or ± 5 Volts
Input Impedance:	1.0 Megohm typical, in parallel with 20 pF. 2.0 Megohms line-line.
Common Mode Rejection:	80dB to 1kHz; 60dB to 50kHz.; typical
Common Mode Range:	± 11 Volts with zero normal-mode input
Overvoltage Protection:	± 25 -Volt transients with power applied; ± 45 Volts with power removed

Transfer Characteristics:

Quantizing Resolution:	24 Bits																		
Sample Rate:	2,000 to 200,000 samples per second.																		
Oversampling Factor:	2-50ksps: x128; 50-100ksps: x64; 100-200ksps: x32																		
DC Accuracy: (Mean composite error after autocalibration)	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th rowspan="2">Input Range</th> <th rowspan="2">Midrange (Zero) Accuracy</th> <th colspan="3">Gain Accuracy at Fsamp</th> </tr> <tr> <th>2-4ksps</th> <th>4-15ksps</th> <th>15-200ksps</th> </tr> </thead> <tbody> <tr> <td>$\pm 5V$</td> <td>$\pm 0.3mv$</td> <td>$\pm 0.9\%$</td> <td>$\pm 0.3\%$</td> <td>$\pm 0.1\%$</td> </tr> <tr> <td>$\pm 2.5V$</td> <td>$\pm 0.1mv$</td> <td>$\pm 0.9\%$</td> <td>$\pm 0.3\%$</td> <td>$\pm 0.1\%$</td> </tr> </tbody> </table>	Input Range	Midrange (Zero) Accuracy	Gain Accuracy at Fsamp			2-4ksps	4-15ksps	15-200ksps	$\pm 5V$	$\pm 0.3mv$	$\pm 0.9\%$	$\pm 0.3\%$	$\pm 0.1\%$	$\pm 2.5V$	$\pm 0.1mv$	$\pm 0.9\%$	$\pm 0.3\%$	$\pm 0.1\%$
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Bandwidth (-3dB)	DC to typically 49 percent of selected sample rate for sample rates to 100KSPS, or to 35 percent of sample rate from 100kSPS to 200KSPS. Typically DC to 70 kHz overall. 0.1dB to 0.45Fsamp; 2-100KSPS; 0.24Fsamp 100-200KSPS.																		
Passband Ripple:	± 0.06 dB maximum																		
Phase Skew:	Typically less than 55ns (0.1-Degree for Fsig = 5kHz), with Fsig/Fsamp < 0.35; channel-channel (board-board for multiboard configurations), excluding noise, with high-frequency image filter.																		
ADC Stopband:	<table> <tr> <td>Sample Rate:</td> <td>Threshold*</td> <td>Rejection*</td> </tr> <tr> <td>2-50KSPS:</td> <td>0.58 Fsamp</td> <td>93dB</td> </tr> <tr> <td>50-100KSPS:</td> <td>0.68 Fsamp</td> <td>90dB</td> </tr> <tr> <td>100-200KSPS:</td> <td>0.78 Fsamp</td> <td>95dB</td> </tr> </table> <p>* Typical values. (Fsamp = sample rate)</p>	Sample Rate:	Threshold*	Rejection*	2-50KSPS:	0.58 Fsamp	93dB	50-100KSPS:	0.68 Fsamp	90dB	100-200KSPS:	0.78 Fsamp	95dB						
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Antialias Filtering:	Each ADC provides linear-phase digital antialias filtering as indicated for "ADC Stopband." A 2-pole Butterworth lowpass analog filter in each channel provides a cutoff frequency of either 40kHz or 270kHz, and suppresses images generated by the digital filter. Optional alternative filter frequencies are available.																		
Dynamic Range:	100dB; typical 2 KSPS to 100 KSPS; 80dB from 100ksps to 200ksps.																		
SINAD:	(Signal to Noise-and-Distortion ratio): 93dB typical to 10 kHz input bandwidth; 85 dB typical to 50 kHz.																		
Interchannel Crosstalk:	-96dB typical to 50kHz																		

Operating Modes and Controls:

Organization:	Two analog input channel groups. All channels in each group operate from a common rate generator that is divided by an independent divisor for each channel in the group. Each group contains one-half of the channels on the board, and can operate either synchronously from a single rate generator, or independently from either of two rate generators.
Sample Rate Generators:	Two independent internal PLL rate generators provide sample rates up to 200 KSPS. The frequency of each generator is controlled a single integer, Setting resolution is 0.2-percent, and setting accuracy is 25 PPM.
External Clock I/O:	A TTL hardware input clock is derived from a 12.8-32.0 MHz external hardware input or from an internal rate generator. Practical TTL cabling limitations may limit the maximum input frequency to less than 30MHz. Multiple boards can be locked to a common clock by daisy-chaining the output clock from each board to the input clock of the next board in the chain. Any number of boards can be daisy-chained together, with a typical propagation delay of 10ns introduced per board. The 'star-configuration' also is supported.
Synchronization:	Sampling of multiple channel groups can be phase-synchronized through software, or each group can be synchronized to an external TTL hardware clock input. Daisy-chained hardware sync inputs and outputs can be used to synchronize sampling among multiple boards.
Data Format:	Software-selectable as either offset binary or two's complement. Width of the data-field is selectable as 16, 18, 20 or 24 bits.
Channel Tags:	A channel tag is appended to each input data value.
Buffer Threshold Flag:	Asserted when the number of samples in the selected buffer exceeds the selected threshold. The threshold can be any integer from zero to 3 FFFEh.
Buffer Access:	The input buffer FIFO is accessed through either of two DMA channels, with both block-mode and demand-mode transfers supported.

PCI Compatibility:

Conforms to PCI Specification 2.3: D32, 33MHz, universal (3.3V/5V) signaling.
Supports "plug-n-play" initialization.
Single multifunction interrupt on INTA#.
Two-Channel DMA as bus master in block and demand modes.

Power Requirements:

+5.0 VDC \pm 0.25 VDC at 0.70 Amps typical at 8KSPS; 0.85 Amps, maximum.

Mechanical Characteristics:

Height: 23.3 mm (0.92 in)
Width: 94.0 mm (3.78 in)
Depth: 95.9 mm (3.70 in).

Environmental Specifications:

Ambient Temperature Range:	Operating: Standard: 0 to +65 degrees Celsius inlet air Extended: -40 to +80 degrees Celsius inlet air Storage: -40 to +85 degrees Celsius.
Relative Humidity:	Operating: 0 to 80%, non-condensing Storage: 0 to 95%, non-condensing
Altitude:	Operation to 10,000 ft.
Cooling:	Conventional convection cooling; 100 LFPM

Ordering Information:

Specify the basic product model number PC104P-24DSI12-4-16SDI.

SYSTEM I/O CONNECTIONS

I/O CONNECTOR PIN ASSIGNMENTS

ROW-A		ROW-B	
PIN	FUNCTION	PIN	FUNCTION
1	INPUT RETURN	1	INPUT RETURN
2	INPUT RETURN	2	INPUT RETURN
3	INP CHAN 00 LO	3	(No connect) *
4	INP CHAN 00 HI	4	(No connect) *
5	INPUT RETURN	5	INPUT RETURN
6	INPUT RETURN	6	INPUT RETURN
7	INP CHAN 01 LO	7	(No connect) *
8	INP CHAN 01 HI	8	(No connect) *
9	INPUT RETURN	9	INPUT RETURN
10	INPUT RETURN	10	INPUT RETURN
11	INP CHAN 02 LO	11	(No connect) *
12	INP CHAN 02 HI	12	(No connect) *
13	INPUT RETURN	13	INPUT RETURN
14	INPUT RETURN	14	INPUT RETURN
15	INP CHAN 03 LO	15	(No connect) *
16	INP CHAN 03 HI	16	(No connect) *
17	INPUT RETURN	17	INPUT RETURN
18	INPUT RETURN	18	INPUT RETURN
19	(No connect) *	19	(No connect) *
20	(No connect) *	20	(No connect) *
21	INPUT RETURN	21	INPUT RETURN
22	INPUT RETURN	22	INPUT RETURN
23	(No connect) *	23	(No connect) *
24	(No connect) *	24	(No connect) *
25	VTEST RETURN	25	INPUT RETURN
26	VTEST	26	INPUT RETURN
27	DIGITAL RETURN	27	DIGITAL RETURN
28	DIGITAL RETURN	28	DIGITAL RETURN
29	(No connect) *	29	(No connect) *
30	EXT CLK INP	30	EXT CLK OUT
31	DIGITAL RETURN	31	DIGITAL RETURN
32	DIGITAL RETURN	32	DIGITAL RETURN
33	(No connect) *	33	(No connect) *
34	EXT SYNC INP	34	EXT SYNC OUT

* "No-connect" pins should be open (unconnected) at the remote end of the system I/O cable.

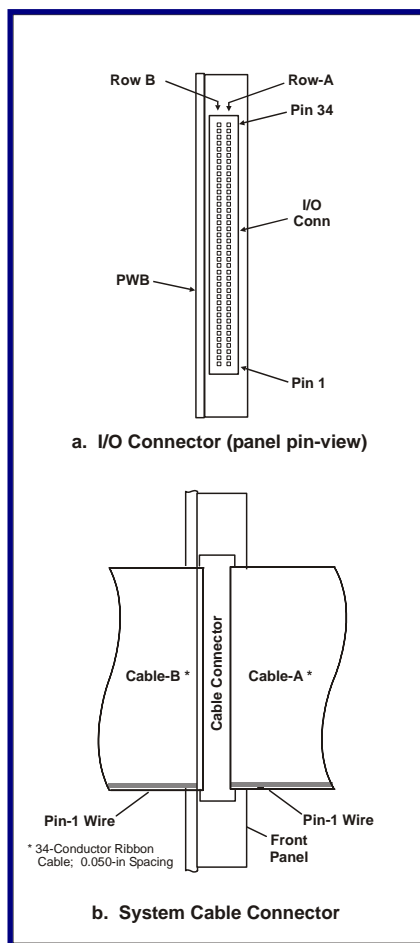


Figure 2. System I/O Connector

System Cable Mating Connector:

68-pin 0.050" Subminiature connector: with metal shield:
AMP #749621-7 or equivalent.

I/O Connector Installed on Board (Ref):

Amp # 787170-7

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