PC104P-16SDI6

16-Bit, 6-Channel Sigma-Delta Analog Input PMC Board

With 220 KSPS Sample Rate per Channel, and 2 Independent Clocks
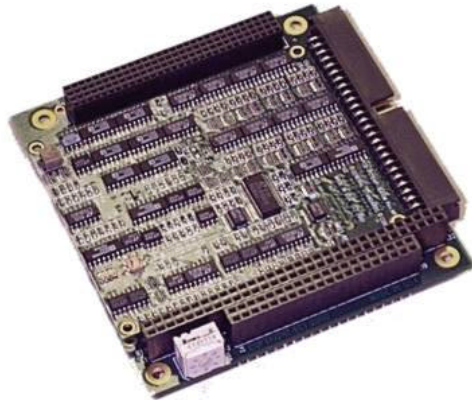
Features Include:

- Sigma-Delta Conversion; No External Antialiasing Filters Required

- High Effective Sampling Rate; 64 Times the Effective Rate of Successive Approximation

- Converters Operating at the Same Conversion Rate

- Integral Antialiasing Input Filters Reject Out-of-Band Interference Components

- Completely Software Configurable; No Field Configuration Jumpers

- Six 16-Bit Analog Input Channels; Dedicated Sigma-Delta Converter per Channel

- Sample Rates Selectable from 5K to 220K Samples per Second per Channel

- Two Independent Sample-Rate Generators; Adjustable with 0.2 Percent Resolution

- Low Noise; Less than 60μVRMS on ±1.25 Volt Input Range

- 64K-Sample FIFO Buffer. All Data is Channel-Tagged.

- Harmonic Sampling Supported, with Clocking Ratios Between Channels from 1 to 32

- Auto calibration Uses Hardware Correction; No missing Codes Introduced

- Integral Shield Assures Minimum Susceptibility to Radiated Noise in PMC Environments

- Single-width PMC Form Factor

- WinNT™, Win2000™, WinXP™, WinME™, Win98™ Drivers are available.

- VxWorks™, Linux 2.2™, LabView™ & Mercury™ Drivers are available.

Applications Include:

- ✓ Acoustics Analysis
- ✓ Analog Inputs
- ✓ Data Acquisition Systems

- ✓ Voltage Measurement
- ✓ Process Monitoring
- ✓ Industrial Robotics

- ✓ Automatic Test Equipment
- ✓ Audio Waveform Analysis
- ✓ Environmental Test Systems

Overview:

The 6-channel PC104P-16SDI6 analog input board provides high-density precision 16-bit analog input resources in a single-width PMC form factor. Optimized for flexibility and performance, the board is ideal for a wide variety of applications, ranging from precision voltage measurements, to the analysis of complex audio signals and waveforms. Each of the six sigma-delta analog input channels can be controlled by either of two independent sample clocks, and multiple channels can be harmonically locked together. Sample rates are adjustable from 5 KSPS to 220 KSPS, and the input range is software selectable as ±1.25V, ±2.5V, ±5V or ±10V. Internal auto calibration networks permit periodic calibration to be performed without removing the board from the system.

Functional Description:

A PCI interface adapter provides the interface between the controlling PCI bus and the internal local controller through a 32-bit local bus (Figure 1). Each of the six input channels contains an input buffer, an adaptive digital-image filter, and a dedicated sigma-delta A/D converter (ADC). The inputs can be configured for either differential or single-ended operation, or an internal voltage reference can be applied to all channels to support selftest operations and auto calibration. Gain and offset trimming of the input channels is performed by calibration DAC's that are loaded with channel correction values during auto calibration. The use of calibration DAC's eliminates the missing codes that occur when analog input channels are calibrated exclusively in the digital domain.

Each ADC contains a digital antialiasing filter that rejects out-of-band signals above approximately 48 percent of the selected sample rate. Lowpass analog input filters remove those interference signals that fall within the harmonic images of the digital filter, the first of which occurs at 64 times the sample rate.

Two independent sample-rate clock generators are individually adjustable from 8 MHz to 16 MHz, and are divided down within the local controller to provide individual channel sample rates from 5 KSPS to 220 KSPS. Conversion data from all active channels is transferred to the PCI bus through a 64K-sample data buffer that has a software-controlled threshold for generating interrupt requests.

Multiple channels can be synchronized to perform synchronous sampling, either by a software command, or by external hardware sync and clock input signals. Multiple boards can be daisy-chained together for synchronous operation from a common clock.
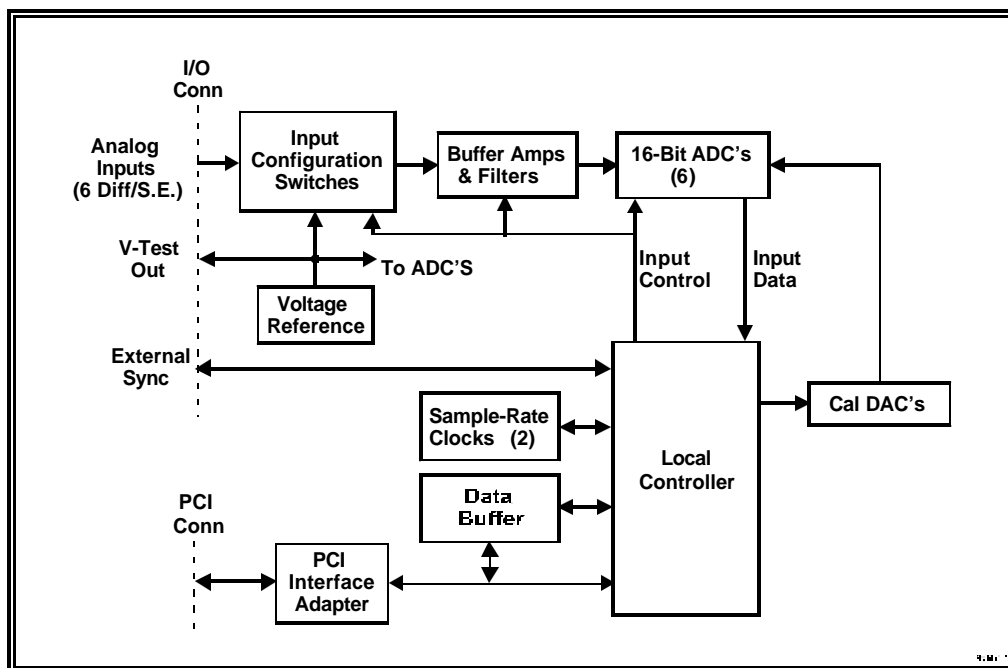
Figure 1.   PC104P-16SDI6; Functional Organization

The board is functionally compatible with the IEEE PCI local bus specification Revision 2.1, and supports the "plug-n-play" initialization concept. System input/output connections are made at the front panel through a high-density 40-pin dual-ribbon connector. Power requirements consist of +5 VDC, in compliance with the PCI specification, and operation over the specified temperature range is achieved with conventional air cooling.

ELECTRICAL SPECIFICATIONS

At +25 ^{O}C, with specified operating voltages.

❑ Input Channel Characteristics:

Configuration:	6 input channels, software controlled as differential or single-ended. Optional 2-channel and 4-channel configurations available.
Voltage Range:	Software Configurable as ±1.25 Volts, ±2.5 Volts, ±5 Volts or ±10 Volts
Input Impedance:	1.0 Megohm typical, in parallel with 20 pF. 2 Megohms line-line.
Common Mode Rejection:	80 dB, DC-60 Hz (Differential mode)
Common Mode Range:	±10 Volts with zero normal-mode input
Offset Voltage:	±0.6 millivolts, maximum
Noise:	1.5LSB-RMS on all ranges, 10Hz-100KHz, typical.
Overvoltage Protection:	±30-Volt transient with power applied; ±15 Volts with power removed

❑ Transfer Characteristics:

Resolution:	16 Bits (0.0015 percent of FSR)
Sample Rate:	5,000 to 220,000 samples per second per channel
Oversampling Factor:	x64

DC Accuracy:
(Maximum composite error)

Range	Midscale Accuracy	±Fullscale Accuracy
±10V	±1.2mv	±5.2mv
±5V	±1.1mv	±3.1mv
±2.5V	±0.9mv	±2.2mv
±1.25V	±0.8mv	±1.5mv

Small Signal Bandwidth:	DC to approximately 48 percent of the selected sample rate
Power Bandwidth:	DC to $2*10^6$ Hz-Vpp minimum. Accepts 100kHz input at 20 VPP.
Crosstalk Rejection:	84 dB typical, DC-10 kHz
Antialias Filtering:	Each ADC provides internal digital antialias filtering at approximately 48 percent of the selected sample rate. This digital filter is supported by a multi-pole analog filter that rejects interference at the harmonic images of the digital filter. The cutoff frequency of the analog filter in each channel is optimized automatically in response to the selected sample rate.
Integral Nonlinearity:	±0.003 percent of FSR, typical
Differential Nonlinearity:	±0.0015 percent of FSR, maximum
Total Harmonic Distortion:	84 dB typical, from DC to 40 percent of sample rate

❑ Operating Modes and Controls

Organization:
Two 3-channel analog input groups, and two sample rate generators. Each channel group can operate from either rate generator. The sample rate for each individual channel is selected by dividing the frequency of the assigned rate generator by any integer from 1 through 32.

Sample Rate Generators:
Two independent internal rate generators, each adjustable from 16-32 MHz, are divided by 128 to provide two independent sample rate sources. Subsequent division by an integer from 1 to 32 for each channel provides sample rates from 3.9 KSPS to 250 KSPS. (Specified performance is guaranteed only within the range from 5 KSPS to 220 KSPS). Settling time when changing frequencies is approximately 20 ms, and settling completion is selectable as an interrupt event. Setting resolution is 0.2 percent or less, and setting accuracy is ±0.08 percent.

External Clock I/O:
An LVDS hardware output clock can be derived either from a 16-32 MHz LVDS external hardware input clock or from an internal rate generator. The external clock input can be selected as the rate generator for any or all channels. .

Multiple boards can be locked to a common clock by daisy-chaining the output clock from each board to the input clock of the next board in the chain. This requires a split I/O cable. As many as eight boards can be daisy-chained together.

Synchronization:
Sampling can be synchronized within each channel group through software, or each group can be synchronized to an external LVDS hardware sync input. By using the daisy-chain configuration described for External Clock I/O, hardware sync inputs and outputs can be used to synchronize the sampling among multiple boards.

Harmonic Sampling:
Harmonic sampling ratios are implemented by adjusting the sample rates of channels within a group to specific fractions of the assigned rate generator frequency. (See Sample Rate Generators).

Data Format:
Software selected as either offset binary or two's complement

Channel Tags:
Each input data value is appended with a 2-bit channel identification tag.

Buffer Size Register:
Contains the total number of samples present in the input data buffer.

Buffer Threshold Flags:
A threshold flag is asserted when the number of samples in the input data buffer equals or exceeds the selected threshold. The buffer threshold can be any integer from 0000 to FFFEh.

AUTOCALIBRATION

During auto calibration, all input channels are calibrated to a precision internal voltage reference. Auto calibration occurs automatically during initialization, and can be invoked at any time after initialization by asserting a single control bit. Once initiated, auto calibration runs to completion without further involvement of the host, and has a duration of approximately 2-5 seconds. Completion of auto calibration is selectable as an interrupt event.

PCI INTERFACE

❑ **Compatibility:**   Conforms to PCI Specification 2.1, with D32 read/write transactions.
Supports "plug-n-play" initialization.
Provides a single multifunction interrupt.
Supports FIFO DMA transfers as bus master.

❑ **Board Control and Data Registers (D32 Access)**

Board Control/Status Register:	Determines the principal operating mode.
Rate Generator Registers:	Select rate generator frequencies.
Channel Control Registers:	Control the clock sources and sample rates for all input channels.
Input Data Buffer:	64K by 18-Bit FIFO buffer.
Buffer Threshold:	Selects the input data buffer threshold.
Interrupt Control:	Interrupt source control and status.

❑ **Analog Input Buffer**

Analog input data is read through a 64K-sample FIFO buffer as a 19-Bit data field for each input sample. The data field contains a 16-Bit conversion value and a 2-Bit channel tag. A threshold flag occurs when the associated buffer contains a number of data samples that exceeds a software-selected threshold from 0000h to FFFEh, and can be used to generate empty and full flags.

MECHANICAL AND ENVIRONMENTAL SPECIFICATIONS

❑ **Power Requirements**

+5VDC ±0.2 VDC at 1.0 Amps, maximum, 1.1 Amps typical
Power Dissipation: 7.0 Watts maximum; 5.5 Watts typical

❑ **Physical Characteristics** (Overall, excluding spacers)**:**

Height: 23.3 mm (0.92 in)
Width: 94.0 mm (3.78 in)
Depth: 95.9 mm (3.70 in)

❑ **Environmental Specifications**

Ambient Temperature Range: Operating: 0 to +70 degrees Celsius *
                                Storage: -40 to +85 degrees Celsius

                                  *Temperature of inlet cooling air.

Relative Humidity: Operating: 0 to 80%, non-condensing
                        Storage: 0 to 95%, non-condensing

Altitude: Operation to 10,000 ft.
Cooling: Conventional convection cooling

❑ **Cooling Requirements**

Conventional air cooling; 200 LPFM (typical mezzanine environment).

ORDERING INFORMATION

Specify the basic product model number (PC104P-16SDI6), followed by an option suffix "-A", as indicated below. For example, model number PC104P-16SDI6-6 describes a board with 6 input channels.*

Optional Parameter	Value	Specify Option As:
Number of Input Channels:	2 Channels	A = 2
	4 Channels	A = 4
	6 Channels	A = 6

*Call for availability of other configurations.

SYSTEM I/O CONNECTIONS

Table 1. System Connector Pin Functions

| P5, ROW-A (Cable-A) PIN	SIGNAL	P5, ROW-B (Cable-B) PIN	SIGNAL
1	EXT CLOCK INPUT LO	2	EXT CLOCK OUTPUT LO
3	EXT CLOCK INPUT HI	4	EXT CLOCK OUTPUT HI
5	GROUND	6	GROUND
7	GROUND	8	GROUND
9	EXT SYNC INPUT LO	10	EXT SYNC OUT LO
11	EXT SYNC INPUT HI	12	EXT SYNC OUT HI
13	VTEST RETURN	14	INPUT RETURN
15	VTEST	16	INPUT RETURN
17	INPUT 02 LO	18	INPUT 05 LO
19	INPUT 02 HI	20	INPUT 05 HI
21	INPUT RETURN	22	INPUT RETURN
23	INPUT RETURN	24	INPUT RETURN
25	INPUT 01 LO	26	INPUT 04 LO
27	INPUT 01 HI	28	INPUT 04 HI
29	INPUT RETURN	30	INPUT RETURN
31	INPUT RETURN	32	INPUT RETURN
33	INPUT 00 LO	34	INPUT 03 LO
35	INPUT 00 HI	36	INPUT 03 HI
37	INPUT RETURN	38	INPUT RETURN
39	INPUT RETURN	40	INPUT RETURN
41	NO CONNECT	42	NO CONNECT
43	NO CONNECT	44	NO CONNECT
45	NO CONNECT	46	NO CONNECT
47	NO CONNECT	48	NO CONNECT
49	NO CONNECT	50	NO CONNECT
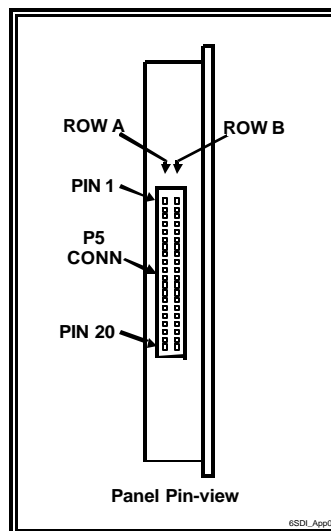
Figure 2. System Input/Output Connector

System Mating Connector:
Rugged 50-pin 0.050" dual-row connector with metal shell.   Amp 1-103311-0

Board connector mates with cable connector AMP part# 1-746285-0

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