

MCP500

3U VPX Many-Core Processor Single Board Computer

Features

- Tiler[®] TILEPro64™ 700MHz processor (64 general purpose processor cores for compute-intensive applications)
- 2x Four-lane PCIe interface (Gen1 support)
- Four banks of 512MBytes DDR2 800 SDRAM
- 2x 10Gbps XAUI connections for interfacing to external 10GbE 10GBASECX4 devices
- RS-232 UART
- User-selectable boot options, including host boot via the PCIe on board boot ROM*
- C/C++ Programming model
- Supports Linux, SMP Linux and VxWorks[®]
- Standard tool chain based on Eclipse and GNU
- Convection and conduction cooled variants
- Host Operating System support for Linux

The MCP500 is a 3U VPX-REDI Single Board Computer based on the Tiler processor and is part of the VPXcel3 product family. This processor delivers the industry's highest performance processing for demanding applications in image processing and networking by exploiting the natural parallelism inherent in applications such as video (pixel and frame parallel), network (session and packet parallel), and wireless (channel parallel).

The MCP500 utilizes the System-On-Chip processor which integrates a scalable interconnect to provide high bandwidth and extremely low latency communication paths to multiple external interfaces such as external DDR2 memory, 10Gb XAUI inter-

faces and PCI Express for optimized use in VPX systems. The dual x4 PCIe interface is designed to provide a dedicated communications path to other single board computers and I/O cards in order to build complex systems.

The TILEPro64 device is fully programmable via a standard ANSI C and C++ environment, achieving the performance of an ASIC in a software programmable solution, reducing development time and enabling a faster time-to-market.

The MCP500 is available in both convection and conduction cooled variants.

* During the development phase, users can create their own boot images and program the ROM to boot from these (Requires Tiler MDE license and tools).



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Specifications

Processor

- Tiler TILEPro64 Processor at 700Mhz (8 X 8 grid general purpose processor cores)
- 32-bit VLIW processors with 64-bit instruction bundle
- 3-deep pipeline with up to 3 instructions per cycle
- 5.6 MBytes of on-chip cache
- Up to 443 billion operations per second (BOPS)
- 37 Tbps of on-chip mesh interconnect enables linear application scaling
- 200 Gbps memory bandwidth with four 64-bit DDR2 controllers with ECC

Memory

- 2 GBytes of on-board DDR2 memory
- 16 MBytes of write protect flash
- I2C ROM for storing boot image firmware

Interfaces

- Two 10GbE XAUI interfaces
- Two 4-lane PCIe Gen 1
- 1 x RS232

Power

- 20-60 W Depending on load and temperature. Idle tiles can be put into low-power sleep mode.

Physical

- Convection or conduction cooled
- Temperature: -40 to +75° C at cold wall
- Weight: 530g
- Shock: 40g
- Vibration: 0.1g²/Hz

Dimensions

- Conforms to 3U VPX standard

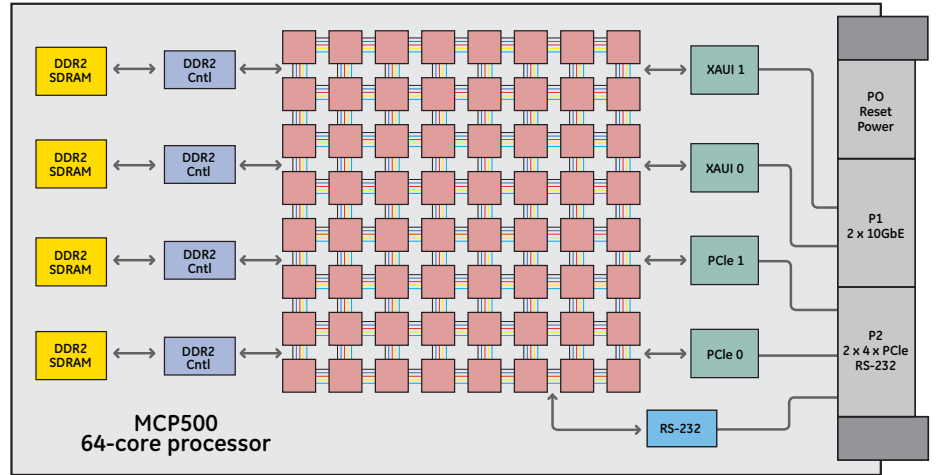
Hardware Support

- Optional rear transition module for development
- Power, status and I/O LED's
- Reset button

Software Support

- C/C++ programming environment
- Support for Linux

Block Diagram



About GE Intelligent Platforms

GE Intelligent Platforms, a General Electric Company (NYSE: GE), is an experienced high-performance technology company and a global provider of hardware, software, services, and expertise in automation and embedded computing. We offer a unique foundation of agile, advanced and ultra-reliable technology that provides customers a sustainable advantage in the industries they serve, including energy, water, consumer packaged goods, government and defense, and telecommunications. GE Intelligent Platforms is a worldwide company headquartered in Charlottesville, VA and is part of GE Home and Business Solutions. For more information, visit www.ge-ip.com.

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