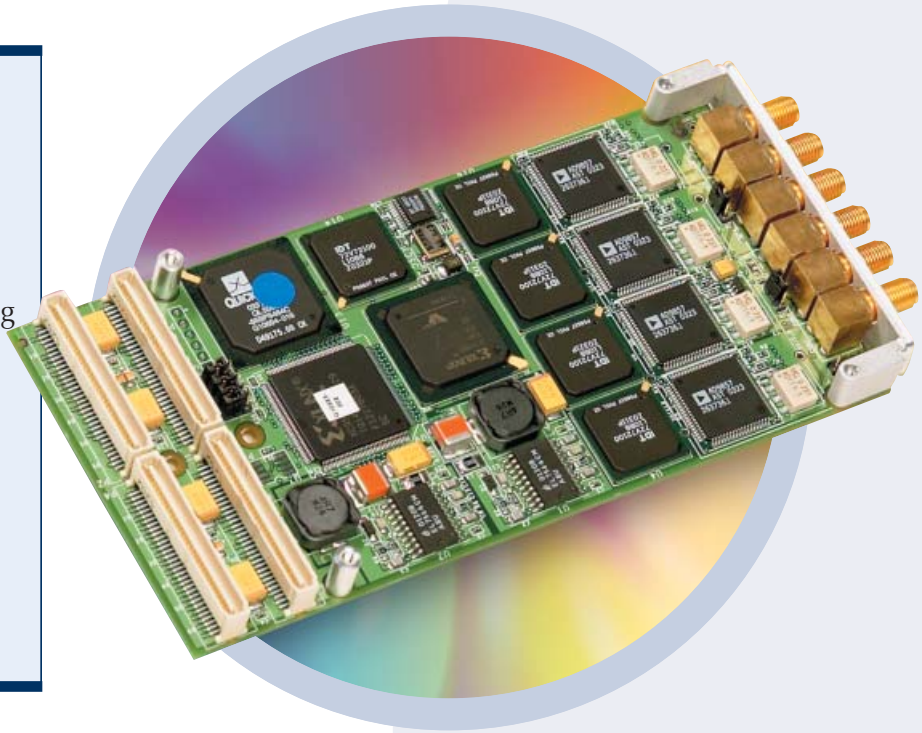
ICS-564

High Performance DAC PMC Module

- Designed for communications, radar and test & measurement applications
- 4 x 200 MHz DAC outputs
- Up to 40 MHz signal bandwidth
- Quadrature modulation, single-tone DDS and interpolating DAC operating modes
- 2 MBytes onboard memory storage
- User programmable 1 million gate FPGA
- Uncommitted Pn4 user I/O PMC interface
- 64-bit, 66 MHz PCI DMA interface



ICS
SENSOR PROCESSING

Designed for communications, radar and test and measurement applications, the ICS-564 PMC module combines unsurpassed DAC technology with industry-leading DSP expertise to provide an efficient combination of cost, size and performance in a single PMC site.

The ICS-564 PMC module consists of four 14-bit DACs, each performing conversions at up to 200 MHz. Each DAC includes a quadrature digital upconverter for programmable complex modulation of a baseband signal, ensuring data can be supplied at the baseband rate. Programmability and ease of operation make the board ideal for radio or radar transmit applications. Up to four signals can be transmitted simultaneously.

The ICS-564 also offers 2 MBytes onboard memory storage together with a fast PCI 2.2 64-bit, 66 MHz DMA interface, as well as 64 user programmable I/O via Pn4.

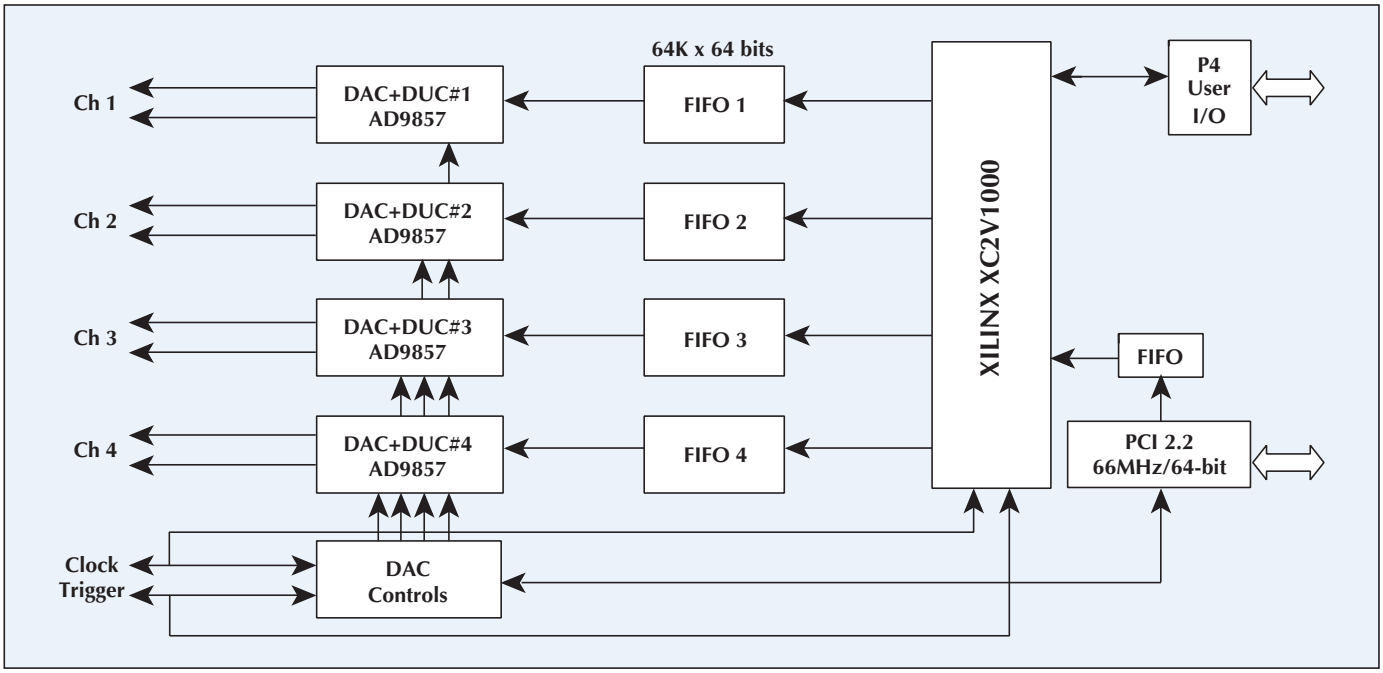
The ICS-564 is ideally suited for applications in military communications, 3G and 4G cellular base station development, signal intelligence, wireless test and measurement and satellite ground stations.

FEATURES

- Four analog output channels
- 14-bit DAC resolution
- SMA coaxial connectors
- 50 Ohm input impedance
- Maximum conversion rate
  - 200 MHz/ch, four channels simultaneous
- Minimum conversion rate
  - 2 MHz/ch, four channels simultaneous
- Transformer coupled outputs
- Full scale output
  - 0 dBm (0.63 Vpp) into 50 Ohms
- Quadrature modulation, interpolating DAC, single tone operating modes
- Programmable interpolation from 4 to 252, in steps of four
- Maximum bandwidth (at 200 MHz conversion rate)
  - 40 MHz (quadrature modulation mode)
  - 20 MHz (interpolating DAC mode)
- Minimum bandwidth (quadrature modulation mode)
  - 634.9 kHz (all four channels) @ 200 MHz conversion
  - 3.174 kHz (all four channels) @ 1 MHz conversion
- Sinewave clock, LVTTL trigger inputs. External trigger sampling occurs following rising edge. Trigger must remain high for at least one clock cycle.
- > 63 dB SFDR @ 20 MHz signal, 200 MHz conversion spurious free dynamic range
- 2 MBytes onboard storage
- FPGA Type
  - Xilinx XC2V1000 (1 million system gates)
- PCI Mezzanine Card compatible with IEEE P1386.1
- PCI 2.2 64-bit, 66 MHz PCI bus interface
- 64 user programmable I/O via Pn4 connector

General

- 0 to +50 degrees celsius operating temperature
- -40 to +85 degrees celsius storage temperature
- 95% non-condensing humidity
- ~ 200 linear feet per minute (lfpm) cooling
- Current draw
  0.8 A @ +5 V
  3.0 A @ +3.3 V



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