

AT2-5800 IP Packet Processor Blade & RTM

Intelligent High-Performance Dual OCTEON™ IP Packet Processor Blade

Features

Interface Support

- Supports two intelligent high-performance Cavium OCTEON™ Plus 16-core CN5860-SCPs (Secure Communications Processors) with up to 750 MHz
- SPI-4.2 Interface for processor interconnection
- Up to 8 Gbyte of high-speed DDR2 packet memory per CN5860 processor
- 10x1 Gigabit Ethernet (GbE) copper or fiber SFP ports via Rear Transition Module (RTM) I/O
- Up to 16 Mbyte RAM of Persistent Memory
- Redundant 1 GbE base interface
- Redundant 10 GbE fabric interface
- Designed for NEBS compliance

PICMG® Compliance/Form Factor

- PICMG 3.0 R2.0 ECN002 compliant
- PICMG 3.1 Option 9 compliant

Firmware/Software Support Available

- IPMC Management Sub-System
- Wind River PNE-LE Carrier Grade Linux® Operating System
- U-Boot, LSP, POST

Product Reliability

- Telco-grade reliability calculated via Telcordia SR 332 Issue 1
- Technical support for OEM customers and resellers

Network Access/Edge Applications

- Session Border Controller (SBC)
- Firewall
- Secure Access Gateway
- Network Address Translation (NAT)
- Traffic Management
- Router/Switch

The AT2-5800, based on two high performance OCTEON™ Plus multi-core processors, is ideal for application services such as 3G/4G Wireless and IPTV that demand wire-speed IP packet processing. By enabling data and control plane services in the same form factor, the AT2-5800 provides efficient packet processing as well as significant performance and cost advantages.

The AT2-5800 blade is designed to enable rapid application development using open, modular, highly available systems based on AdvancedTCA architectures. Dual Cavium OCTEON 16-core CN5860-SCP processors @750MHz with 2 Mbyte of shared L2 cache memory provide up to 10 Gbit/s line-speed core processing for network Layers 2-7. With dual 16-core processors, this blade has 32 MIPS64 cores for high-speed packet processing.

To optimize application performance, the CN5860-SCP supports a dual-issue, five-stage pipeline and optimized latencies as well as auto instruction pre-fetching and advanced data pre-fetching features to minimize memory delays.

This packet processor AdvancedTCA blade can be configured to enable a wide variety of applications. Up to 16 Gbyte (8 Gbyte per processor) of high-speed, low-latency DDR2 memory is implemented as packet memory.

Rear Transition Module (RTM) I/O

I/O operations are provided through a RTM. For application flexibility, the AT2-5800 supports multiple RTM configuration options including any combination of up to 10 ports of IEEE 1000BaseT,

1000BaseSX, or 1000BaseLX via Small Form Factor Pluggable (SFP) transceivers.

Software

The AT2-5800 software implementation is a comprehensive development package designed to improve time-to-revenue. The software development package is optimized to simplify application integration for multi-core processor development environments.

Intelligent Platform Magement Interface (IPMI)

Designed for high availability applications, the AT2-5800 includes an Intelligent Platform Management Controller and firmware subsystem that provides blade management services compliant with IPMI v1.5 or v2.0. This includes blade level parameters, monitoring voltage and temperature conditions, maintaining system status, and managing hot swap operations.

At its lowest level, the AT2-5800 software includes a Universal Boot loader (U-Boot) and a comprehensive Power On Self Test (POST) embedded in the firmware. U-Boot loads user application code from the network (e.g. TFTP server) or via local Flash memory.

A Linux Support Package (LSP), Application Program Interface (API) and sample application code designed to exercise the AT2-5800 are provided to aid in application development. The Linux Support Package includes Wind River Carrier Grade Linux Operating System (PNE-LE) with Cavium Software Development Kit and user application diagnostics. Other operating systems are available upon request.



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Specifications

Processors

- Dual OCTEON™ Plus CN5860-SCP, 16-core @750MHz

Memory

- Up to 8 Gbyte of DDR2 SDRAM per processor
- Up to 256 Mbyte Flash memory per processor

Front-Panel

- x3 Micro-DB9 interfaces
- x2 1Gigabit Ethernet control plane interfaces
- Status LEDs

Base Interface

- Redundant 1 GbEs (Dual Star)

Fabric Interface

- Redundant 10 GbE XAUIs (Dual Star)

RTM I/O

- Line I/O - 10x 1 GbE via SFP connectors
- Control plane - 2x 1 GbE via SFP connectors

PICMG Compliance/Dimensions

- PICMG 3.0
- PICMG 3.1 Option 9
- 8U single slot AdvancedTCA format
- Height: 12.68 in. (322.25mm)
- Depth: 11.0236 in. (280mm)
- Blade weight: 7.252 lbs (3.289 Kg)
- RTM weight: 1.572 lbs (0.713Kg)

Power Requirements

- 48 VDC
- 200 watts

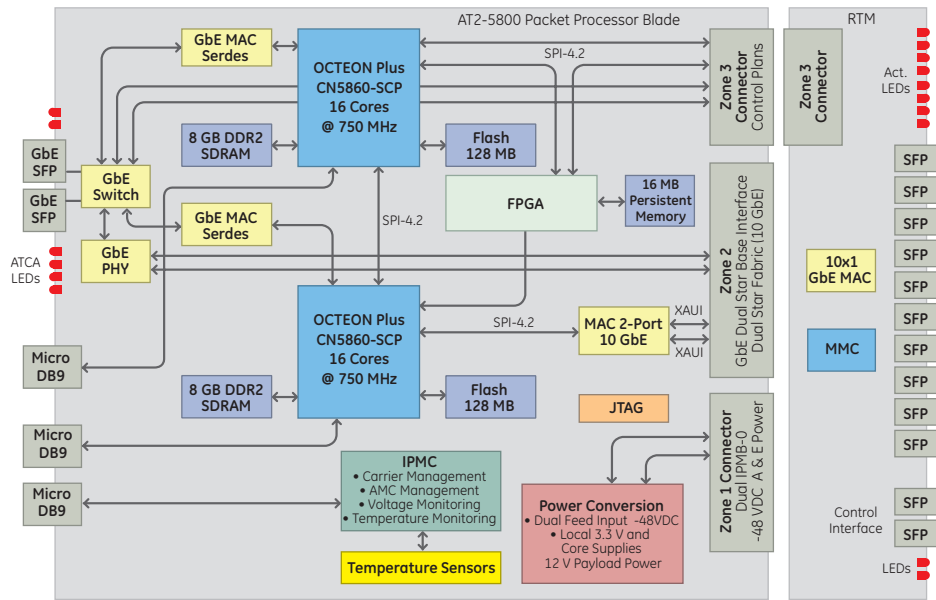
Environmental

- Temperature
 - Operating: 0° to +55 °C
 - Storage -40° to +85 °C
- Relative Humidity
 - Operating: 5% to 95%, noncondensing
 - Storage: 5% to 95%, noncondensing

Regulatory Compliance

- CE Mark
- Emissions
 - FCC 47CFR Part 15 Class A (USA)
 - EN55022: 1998/A1:2000/A2:2003 Class A ITE (EU)
 - EN55024
 - VCCI Class A ITE (Canada)
 - AS/NZ CISPR 22:2002 Class A (Aus. New Zealand)
 - ICES-003 Issue 3 Class A (Canada)
 - VCCI Class A ITE
 - EMC Directive 89/366/ECC
- Immunity
 - EN55024:1998/A1:2001/A2:2003 (EU)
 - EN ETS 300 386
- Safety
 - UL60950-1 (USA)
 - CSA 22.1 no. 60950-1-03 (Canada)
 - EN 60950-1 (EU)
- RoHS 2002/95/EC
- Designed for NEBS compliance

Block Diagram



Ordering Information

85020-204

AT2-5800-10G with dual 16-core CN5860_SCP @ 750MHz processors, 4GB DDR2 per processor, 2 control plane 1000BaseT SFPs; RoHS 6/6

85020-207

AT2-5800-RTM-GbE RTM with 10x1000BaseSX SFP ports, 2 control plane 1000BaseT SFPs; RoHS 6/6

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