VME-3122A Specifications

High-Performance 16-bit Analog-to-Digital Converter (ADC) Board

Features:
- 64 different or single-ended inputs
- 16-bit Analog-to-Digital (A/D) conversion
- Software-selectable conversion rate (100 kHz maximum)
- Program-selectable scanning of 1, 8, 16, 32 or 64 channels
- Continually digitizes selected input channels and stores the results
- Three trigger modes
  - Software trigger
  - External trigger
  - Interval timer trigger
- Three scan modes
  - Autoscan
  - Single scan
  - Random access
- Programmed VME interrupts
- User-programmable interval timer
- Software-programmable gain 1 and 10
- External trigger to synchronize multiple boards simultaneously
- Jumper-selectable A/D ranges of 0 to +5 V, 0 to +10 V, ±2.5 V, ±5 V and ±10 V
- Optional low pass filter
- Overvoltage protected inputs
- 1,024-word data buffer (16-word deep buffer x 64 channels)
- Selectable output coding
- Powers up in autoscanning mode with unity gain

Applications:
- Factory automation and instrumentation
- Process control
- Laboratory instrumentation
- Machine monitoring
- Data acquisition
The board supports the following operating modes, which are described below:

**Trigger Modes**
- Software Trigger
- External Trigger
- Interval Timer Trigger

**Scan Modes**
- Autoscan
- Single Scan
- Random Access

One thousand twenty-four dual-port Data Registers provide storage for continuous scanning of all channels. The trigger and scanning modes are executed automatically at power up, system reset, or are entered under program control. The dual-port registers allow VME access at any time to read the latest stored data.

Channel gain is under software control and can be fixed at x1 or x10 or each channel individually programmed for either gain. Conversion rate is selectable up to 100 kSPS (thousand samples/s). Low pass input filters are available.

### Functional Characteristics

<table>
<thead>
<tr>
<th>Style</th>
<th>Recommended Connecting Component</th>
<th>P3 and P4 I/O Connectors</th>
</tr>
</thead>
<tbody>
<tr>
<td>64-pin IDC</td>
<td>Mating Connector (64-pin)</td>
<td>Panduit 120-964-435</td>
</tr>
<tr>
<td></td>
<td>Strain Relief (For 64-pin Connectors)</td>
<td>Panduit 100-000-072</td>
</tr>
<tr>
<td>96-pin Discrete Wire</td>
<td>Mating Connector (96-pin Discrete)</td>
<td>AMP 925486-1</td>
</tr>
<tr>
<td></td>
<td>Female Crimp Contacts (96-pin Discrete)</td>
<td>AMP 530151-6 (See Note 2)</td>
</tr>
<tr>
<td></td>
<td>Connector Housing (For 96-pin Connectors)</td>
<td>Harting 09 03 096 0501</td>
</tr>
<tr>
<td>96-pin IDC</td>
<td>Mating Connector (96-pin Mass-Terminated)</td>
<td>ERNI 913.031</td>
</tr>
<tr>
<td></td>
<td>0.033-inch Ribbon Cable (96-pin Mass-Terminated)</td>
<td>ERNI 913.049</td>
</tr>
<tr>
<td></td>
<td>Strain Relief Insert (0.033-inch Ribbon Cable)</td>
<td>Harting 09 02 000 9912</td>
</tr>
<tr>
<td></td>
<td>Connector Housing (For 96-pin Connector)</td>
<td>Harting 09 03 096 0501</td>
</tr>
</tbody>
</table>

PC Board I/O Connector Part Number Panduit 101-096-033A Panduit is also known as ITW/Pancon.

#### Notes
1. Latches are located on the cable.
2. AMP crimp tool part number 90301-2.

### Ordering Options

<table>
<thead>
<tr>
<th>Dec. 20, 2007 800-103122-000 A</th>
<th>A</th>
<th>B</th>
<th>C</th>
<th>D</th>
<th>E</th>
<th>F</th>
</tr>
</thead>
<tbody>
<tr>
<td>VME-3122A</td>
<td>–</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

**A = Input Filter Option**
- 0 = No Filter
- 1 = 10 Hz (-3 dB)
- 2 = 50 Hz (-3 dB)
- 3 = 100 Hz (-3 dB)
- 4 = 500 Hz (-3 dB)

**B = Number of Channels Option**
- 0 = 64 Channels High Performance
- 1 = 32 Channels High Performance
- 2 = 16 Channels High Performance

**C = Input Option**
- 0 = Differential Analog Input Channels with 96-pin Nonlatching Connector (See Note 1)
- 1 = Single-Ended Analog Input Channels with 96-pin Nonlatching Connector (See Note 1)
- 2 = Differential Analog Input Channels with 64-pin Latching Connector
- 3 = Single-Ended Analog Input Channels with 64-pin Latching Connector

**DE = 0 (Option reserved for future use)**

**F = Special Sales Order**
- 0 = Standard VME front panel without conformal coating
- 1 = Reserved
- 2 = Standard VME front panel with conformal coating

### Introduction
This product is designed to support 64 channels of differential or single-ended wide range (±250 mV to ±10 V) analog inputs.
VMEbus Compliance: This product complies with VMEbus Specification ANSI/IEEE STD 1014-1987 IEC 821 and 297 with the following mnemonics:

- A32/A24/A16:D16/D8 (EO) DTB Slave
- Interrupter I (1 to 7) ROAK (DYN)
- Interrupter Vector: D08 (O) (DYN)

6U form factor

VME Interrupt: An interrupt request can be generated at the end or middle of a buffer scan. The request can also be initiated after a specific number of samples (1 to 65,535) have been acquired. Response vectors are controlled through Interrupt Vector Registers.

Data Ready Flag: A data ready flag in the CSR is set when the data buffer is filled (endscan) or half-filled (midscan).

Interval Timer: Timed intervals of up to 687 seconds are provided by a programmable interval timer.

Reset Operations: Board reset occurs in response to a system reset or by writing to the Software Reset Address. For programming-free initial operation, a reset operation automatically establishes the following default conditions:

- Autoscanning Mode
- 64-channel block size
- 64-channel data buffer
- Channel Gain = x1
- Rate = 100 kHz conversion

The ADC will go through a calibration cycle on either RESET condition. The calibration cycle takes 41 ms after a RESET operation has been initiated.

PGA: Channel gains of x1 and x10 are selected through a Programmable Gain Amplifier (PGA). PGA gain can be software configured for a single gain on all channels, or it can be controlled in real-time with unique gains assigned for each channel.

Panel Indicator: Program-controlled front panel LED is energized during reset, and is extinguished through the CSR.

Board Identification: A Board Identification Register (BIR) contains the VME-3122A identification code.

Input Characteristics

- Number of Input Channels: 64, 32 or 16 differential or single-ended channels
- Full-Scale A/D Ranges: ±2.5 V, ±5 V, ±10 V, 0 to +5 V, 0 to +10 V; jumper selectable
- Channel Gain: Software configured for x1 or x10
- Full-Scale Input Range: Gain = 1: ±2.5 V to ±10 V Bipolar; 0 to +5 V, 0 to +10 V Unipolar
  - Gain = 10: ±250 mV to ±1 V Bipolar; 0 to +0.5 V, 0 to 1 V Unipolar

Accuracy (% of FSR):

<table>
<thead>
<tr>
<th>Range</th>
<th>+10 V</th>
<th>±5 V</th>
<th>±2.5 V</th>
<th>0 to +5 V</th>
<th>0 to +10 V</th>
</tr>
</thead>
<tbody>
<tr>
<td>x 1</td>
<td>0.015</td>
<td>0.008</td>
<td>0.032</td>
<td>0.014</td>
<td>0.012</td>
</tr>
<tr>
<td>x 10</td>
<td>0.058</td>
<td>0.079</td>
<td>0.126</td>
<td>0.135</td>
<td>0.076</td>
</tr>
</tbody>
</table>

NOTE: Based on an average of 1000 samples

Stability: Temperature drift, per degree Celsius = ±25 PPM (ADC reading) plus ±5 PPM (ADC range) plus ±2.5 µV

Example: For a +7.000 V reading in the ±10 V range:

Temperature drift = ±175 µV +100 µV ±2.5 µV = ±277.5 µV

Input Noise: 

\[(0.4 + 0.3/G) \text{mV}\]; where: \(G = \text{PGA Gain (Noise is independent of filter option)}\)

<table>
<thead>
<tr>
<th>Range</th>
<th>+10 V</th>
<th>±5 V</th>
<th>±2.5 V</th>
<th>0 to +10 V</th>
<th>0 to +5 V</th>
</tr>
</thead>
<tbody>
<tr>
<td>x 1</td>
<td>0.509</td>
<td>0.280</td>
<td>0.191</td>
<td>0.381</td>
<td>0.229</td>
</tr>
<tr>
<td>x 10</td>
<td>0.014</td>
<td>0.015</td>
<td>0.014</td>
<td>0.014</td>
<td>0.014</td>
</tr>
</tbody>
</table>

NOTE: Based on all channels scan for 512 data samples

Input Bias Current (typical/maximum): 50/120 nA

Input Impedance (minimum):

<table>
<thead>
<tr>
<th>Condition</th>
<th>DC-Dif</th>
<th>DC-CM</th>
<th>AC-Dif</th>
<th>AC-CM</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power ON</td>
<td>10 M</td>
<td>100 M</td>
<td>250 K</td>
<td>250 K</td>
</tr>
<tr>
<td>Power OFF</td>
<td>8 K</td>
<td>4 K</td>
<td>8 K</td>
<td>4 K</td>
</tr>
</tbody>
</table>

NOTE: Impedances are provided for no filter differential input option. AC impedance measured at 1 kHz.

Interchannel Crosstalk (DC to 1 kHz):

<table>
<thead>
<tr>
<th>±10 V Range Adjacent Channel</th>
<th>±2.5 V Range Adjacent Channel</th>
</tr>
</thead>
<tbody>
<tr>
<td>80 dB</td>
<td>70 dB</td>
</tr>
</tbody>
</table>

Common-Mode Voltage Range:

\(|V_{CM} + V_{IN}G| \leq 10 \text{ V}\)

Where: \(V_{CM} = \text{the common-mode voltage}\)

\(V_{IN} = \text{the input voltage}\)

\(G = \text{the gain}\)

Common-Mode Rejection: DC to 60 Hz with 350 Ω source imbalance

<table>
<thead>
<tr>
<th>Gain</th>
<th>Min</th>
<th>Typical</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>68 dB</td>
<td>80 dB</td>
</tr>
<tr>
<td>10</td>
<td>76 dB</td>
<td>89 dB</td>
</tr>
</tbody>
</table>

Common-Mode Rejection in the +5 V and ±2.5 V range is a minimum of 66 dB. This can be field-trimmed to the same common-mode rejection as the gain of 1.

Overvoltage Protection:

±35 V, sustained Power On/Power Off

±80 V, transient (1 s maximum)
VME-3122A High-Performance 16-bit Analog-to-Digital Converter (ADC) Board

**Input Filters:** Optional low pass single-pole filters:
-3 dB at 10 Hz
-3 dB at 50 Hz
-3 dB at 100 Hz
-3 dB at 500 Hz

These values apply for differential inputs. Frequency doubles for single-ended (pseudo-differential) applications. The cutoff frequency has a tolerance of ±25 percent. Typical no filter input bandwidth (20 Vp-p) is 40 kHz.

**Common-Mode/Floating Input Protection:** Both sides of each input is pulled to ground through a 22 MΩ resistor.

**Transfer Characteristics**

**Resolution:** 16 bits

**Input Sampling:** Sequential, starting at channel 00

**Input Transfer Function:**

\[ E_{IN} = E_{LO} + E_{FSR} \times \frac{N_{ADC}}{65,536} \]

Where: \( E_{IN} \) = Input Voltage  
\( E_{LO} \) = Lower End of Input Range  
\( E_{FSR} \) = Full-Scale Input Range  
\( N_{ADC} \) = A/D Converter Reading

Example: For a \( N_{ADC} \) value of D99A HEX (55,706 decimal) in the ±10 V range:

\[ E_{IN} = -10 + \left[ 20.000 \times \left( \frac{55,706}{65,536} \right) \right] = +7.000 \]

**A/D Conversion Rate:** 381 to 100 kSPS

**Channel Sample Rate (Maximum):** 100 kSPS  
(100 kSPS ÷ number of channels in scanning block, 1 channel minimum)

**Timed Interval:** 305 µs to 687 s

**Data Coding:** Program selectable as two's complement, or straight/offset binary

**Data Buffer Memory**

**Buffer Size:** 16 to 1,024 contiguous 16-bit data words; program controlled

**Block Size:** 1, 8, 16, 32, or 64 channels; program controlled

**Access Time:**
Nonscanning: 600 ns maximum  
Scanning: 600 ns typical, 1.2 µs maximum  
Maximum access time in scanning mode will occur only when VME access occurs in ADC sample window.

**VME Access:** D8 to or D16

**Availability:** Accessible at any time from the VME. Buffer and block sizes are controlled through a Configuration Control Register (CCR).

**Physical/Environmental Specifications**

**Dimensions:** 6U (4HP) single slot Eurocard form factor

- Height 9.2 in. (233.4 mm)  
- Depth 6.3 in. (160 mm)  
- Thickness 0.8 in. (20.3 mm)

**Power Requirements:**
3.0 A (maximum) at +5 VDC

**Airflow:** Forced air cooling required

**Temperature:**
Operating: 0 to +65° C  
Storage: -40 to +85° C

**Altitude:**
Operating: 0 – 10,000 ft (3,000 m)  
Storage: 0 – 40,000 ft (12,000 m)

**Humidity:**
Operating: relative humidity 0% to 80%, noncondensing

**Input Connectors (P3, P4):** Input connectors P3 and P4 may be ordered as either 96-pin DIN nonlatching or 64-pin DIN latching. The 96-pin nonlatching connectors offer the center row as ground, while the center row ground is not available on the 64-pin latching connector. When using the 64-pin latching connectors in differential mode, the user may jumper E1 and E2 to provide ground on the front panel, this will result in configuring channels 31 and 63 as single-ended. See the Ordering Options C field (Input Option).

**MTBF:** Contact factory

**UIOC® Support**

In a UIOC, the VME-3122A is used as a monitoring device. During initialization, the UIOC programs the VME-3122A to scan all 64 channels and sets the scan mode to Autoscan. Through UCLIO™ language, the user may set programmable channel gains and command the UIOC to acquire data from any or all of the VME-3122A channels. Through a menu-driven calibration process, the user may create and store channel gain and offset correction factors which are automatically used by the UIOC to provide software gain and offset corrections for each channel.

**Trademarks**

All registered trademarks are the property of their respective owners.

**Application and Configuration Guide**

The following Application and Configuration Guide is available from GE Fanuc Intelligent Platforms to assist the user in the selection, specification and implementation of systems based on GE Fanuc Intelligent Platforms’ products.

<table>
<thead>
<tr>
<th>Title</th>
<th>Document No.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Connector and I/O Cable Application Guide</td>
<td>825-000000-006</td>
</tr>
</tbody>
</table>
VME-3122A High-Performance 16-bit Analog-to-Digital Converter (ADC) Board

Figure 1. VME-3122A Functional Block Diagram