GE Fanuc Automation

PMC941
PMC941FX

Network Interface

OPERATORS REFERENCE MANUAL

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Embedded Systems

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Introduction

The GE Fanuc Embedded Systems family of unmanaged switches is designed to address the following needs:

- State-of-the-art Ethernet Switch Fabric
- Implemented in form factors appropriate for embedded, and quasi-embedded applications (e.g., VMEbus, CPCI, PMC and custom)

GE Fanuc Embedded Systems achieves these goals by integrating advanced chip sets (for high performance switching functions) with numerous media front ends (e.g., BNC, Fiber and copper) and flexible management software. A benefit of this approach is that both hardware (e.g., media types, form factor) and software feature sets may be readily tailored to meet special needs within the context of the commercial off-the-shelf (COTS) model to which GE Fanuc Embedded Systems adheres.

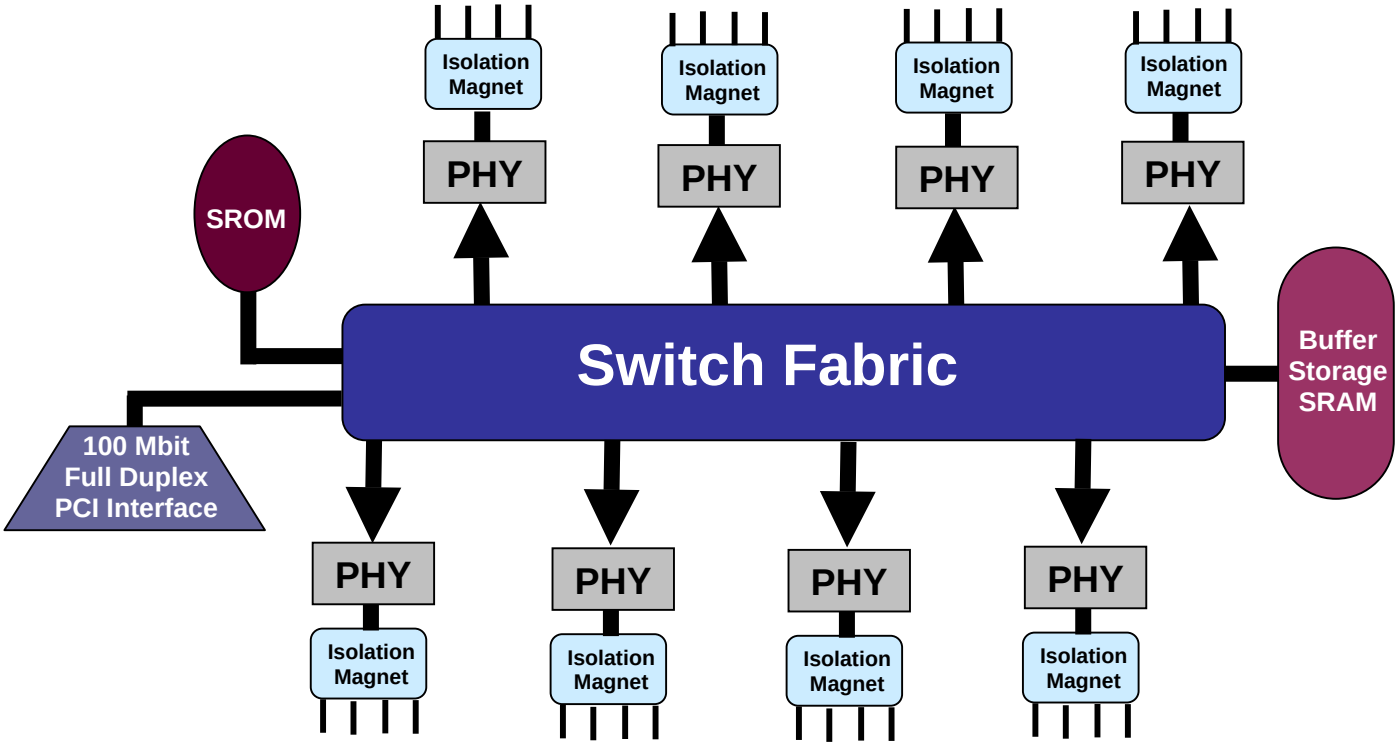
The PMC941/PMC941FX is a fully integrated 8-port Ethernet switch + 1 NIC designed to support the low-cost requirements of unmanaged switch applications and converging networks. The Quality of Service (QoS) technology allows low cost unmanaged switches to carry voice and data traffic without having to compromise the quality of its voice traffic by using the packet prioritization scheme. Packets are prioritized based upon their layer 2 Virtual LAN (VLAN) priority tag or the layer 3 Type-Of-Service/Differentiated Services (TOS/DS) field. This priority can be defined as transmit and/or drop priority. The PMC941 and PMC941FX are identical other than the 4 port front media. The PMC941 has the four front I/O as copper and the PMC941FX has the four ports as fiber.

Key features:

- 8 10/100Mbps auto-negotiating (4 port front access and four port rear)
- On board NIC is connected to the switch at 100 Mbit full duplex
- Full wire speed layer 2 switching on all ports
- 1k MAC address table
- Auto address learning
- Auto address aging Leading edge QoS capabilities, based on 802.1p and IP TOS/DS field
- Enables mixed voice-data networks
- Provides port-based prioritization of packets on 4 ports
  - Input ports are defined to be high or low priority
  - Allows explicit identification of IP Phone ports
- Up to 8 port based VLANs
- Offers port trunking
- Supports port mirroring
- Provides both Full/Half duplex ports
- Flow Control capabilities
  - Back pressure for half-duplex
  - 802.3x flow control for full-duplex

1 Theory Of Operation

The architecture of the switch is illustrated in the below switch block diagram.



Note: The PMC941FX has the four port Fiber in the front vs. the PMC941 which has the copper.

By definition, a Network Switch differs from a hub in that each packet received into the switch is transmitted to the minimum number of ports. This greatly improves the aggregate data rate (i.e., multiple pairs of ports can be involved in data transfer at a single point in time). As each packet arrives at the switch, both the source and destination address of the packet are examined. The source is retained and associated with the arrival port as the location of that device. If the packet is unicast (i.e., destined for a single receiver) and the destination is known, the packet will only be transmitted to the port associated with the destination address. Since the learning is automatic, no operator intervention is needed. As attached workstations (or other network-capable devices) communicate, their locations are learned and traffic can be localized to the port.

In the default configuration the PMC941/PMC941FX switch delivers a fully auto-configuring interconnect. Each port will negotiate speed, and for full duplex, with the connected interface. Once a link has been established, incoming packets are examined and the MAC address is added to the table associated with that port. When the destination address has been associated with a port (from an earlier transmission), the packet is forwarded only to that port. This process is independent for each port, so that the aggregate throughput of the switch fabric is much higher than that of a single channel.

In a case where the destination has not yet been acquired, the packet is sent to all ports (see the ***VLAN*** section for behavior when this option has been configured).

Because the negotiation and learning process is automatic, there is no operator or start-up interaction required. The (SRAM) buffer provides local storage to allow multiple incoming packets with a single destination port. Packets will be sequenced and buffered to avoid data loss. The (optional) QoS offers a mechanism to prioritize traffic.

1.1 Operational Options

The switch fabric has a number of performance operations usually found only in managed switch products. These options include:

- Port based VLAN
- QoS
- Port Speed/Duplex forced configuration

All of these parameters are set via the serial ROM. This can either be programmed prior to manufacturing or configured in the field from the PCI port.

1.2 Port Based VLAN

The switch fabric provides the designer with the ability to define a single port-based VLAN for each of the eight ports. VLAN is individually defined by assigning an ID (value between 0 – 7) for each port.

When packets arrive at an input of the switch, the search engine will determine the VLAN ID for that port. It will then determine which of the other ports also are members of that VLAN by matching their assigned VLAN ID values. The packet will then be transmitted to each port with the same VLAN ID as the source port.

1.3 QoS

QoS provides a new level of capability to unmanaged switch applications with two transmit queues per output port.

The Fabric manages the output transmission queues for all ports of the fabric. Once the destination address search is complete, the packet is inserted into the appropriate output queue. The packet entry into the high or low priority queue is controlled in the IP header by either the VLAN tag information or the TOS field. Each of these priority fields can be used to select the transmission queue priority as well as a packet drop probability. The mapping of the tag and TOS fields to either the high or low priority queue is configured on power-up from the SROM.

The fabric utilizes Weighted Round Robin (WRR), Random Early Drop with In/Out (RED/RIO) bit, and a timestamp method of scheduling packets for transmission. WRR uses an efficient method to ensure that each of the transmission queues gets at least a minimum service level. With two output transmission queues, the fabric will transmit “X” packets from the high priority queue before transmitting “Y” packets from the low priority queue. The “X” and “Y” weights are user-definable. The high priority weight can be set to a value between 0 and 16. The low priority weight is fixed at value 1. If the high priority weight is set to the value 4, then the fabric will transmit 4 high priority packets before transmitting each low priority packet.

The timestamp method of scheduling packets for transmission allows the fabric to offer latency guarantees to high priority packets. This is ideal for voice and video packets that have strict latency requirements. Packets are given a timestamp when they arrive at the input port. Once they are scheduled into a transmission queue, the fabric will keep track of the packets delay time through the chip. Under heavy congestion the timestamp may be utilized to change the order of packet transmission to ensure timely delivery of packets and orderly service of congested queues. The following are exceptions to transmission scheduling:

- Packets with high priority and low drop priority will be transmitted before any in the low priority queue.
- If the high priority delay is => 2ms, then transmit from the high priority queue.
- If the high priority delay is < 1ms and the low priority queue is congested, then transmit from the low priority queue.
- If the high priority delay is < 2ms and the low priority queue is full, then transmit from the low priority queue.

The QoS capabilities of the fabric are enabled by loading the appropriate values in the configuration registers and by either enabling or disabling flow control. To enable QoS of packet transmission, perform the following steps:

1. Select the TOS or VLAN Tag field as the control for packet transmission. The selection is made by using bit 6 of the FCB Buffer Low Threshold (FCBST[6]) register.

2. Select the TOS or VLAN Tag field as the control for IP packet transmission. The selection is made using bit 7 of the Flooding Control (FCR[7]) register.

3. Set the transmission queue weight for the high priority queue in the Transmission Scheduling Control (AXSC[3:0]) register.

4. For half duplex operation, the transmission queueing must be enabled using bit 7 in the Trans-Mission Scheduling Control (AXSC[7]) register.

5. Set the priority mappings from the TOS or VLAN Tag field, to the high or low priority output queue.

When flow control and QoS are enabled the fabric will utilize WRR to schedule packet transmission, and will use either backpressure or 802.3x flow control to handle situations of buffer memory congestion. When flow control is disabled and Qos is enabled, the fabric will use RED/RIO to drop random packets in order to handle situations of buffer memory congestion. In this method, only certain packet flows are slowed down while the remaining incur no impact from the network traffic congestion. RED/RIO bit is a method of handling traffic congestion in the absence of flow control mechanisms. When flow control is enabled all devices that are connected to a switch node that is exercising flow control are effectively unable to transmit, even nodes that are not directly responsible for the congestion problem. RED/RIO allows traffic to continue flowing into ports on a switch and randomly drops packets with different probabilities based upon each packet's priority markings. As the switch congestion increases, the probability of dropping an input packet increases. As congestion decreases, the probability of dropping an input packet decreases. In this manner, only traffic flows that have had packets dropped will be affected by the congestion. Other traffic flows will incur no effect.

1.4 Port Configuration

By setting parameters in the SROM each port can be individually configured in speed (i.e., 10Mbs or 100Mbs) and duplex (i.e., full or half).

2 Handling and Installation

2.1 Handling Precautions

Electronic assemblies use devices that are sensitive to static discharge. Observe anti-static procedures when handling these boards. All products should be in an anti-static plastic bag or conductive foam for storage or shipment. Work at an approved anti-static workstation when unpacking boards.

2.2 Unpacking and Verification

GE Fanuc Embedded Systems products are shipped in individual, reusable shipping boxes. When receiving the shipping container, inspect it for any evidence of physical damage. If the container is damaged, request that the carrier's agent be present during the unpacking of individual boxes and the inspection of each unit.

Remove the PMC941/PMC941FX card from the shipping box and anti-static packaging. Verify that it is not damaged and that all items are present by referring to the packing list. Each card is shipped with a PMC Assembly.

2.3 Installation

The PMC941/PMC941FX consumes a single PMC Slot.

> ***Note***: There are no on-board user-configured jumpers for this product.

Locate the PMC slot in the chassis into which the Switch will be installed.

Remove power from the chassis.

Observing proper anti-static procedures, insert the Switch Assembly into the chassis. Use the ejector handles to ensure the card is fully seated into the backplane.

The chassis may now be powered up.

3 Front/Rear Panel Connections & Indicators

The front panel of the PMC941/PMC941FX has four Flush RJ-45 connectors that can interface directly to any NIC. The PMC941/PMC941FX also has four ports which route to the rear on the J4 connector of the PMC (see the ***I/O Pen Assignments*** section for pin out for the J4 connector).

3.1 Network Connections

There is a single PCI/Ethernet chip which mates to the PCI Bus. This allows the host to connect directly to the switch fabric without any external cables. This port can also be used as a second interface Ethernet in addition to the host. The network interface runs at the 100Mbit full duplex into the switch fabric.

> ***Note***: Connecting to another Ethernet HUB or SWITCH: A "crossover" cable must be used, or the connection must be to the "uplink" port of the hub or switch.

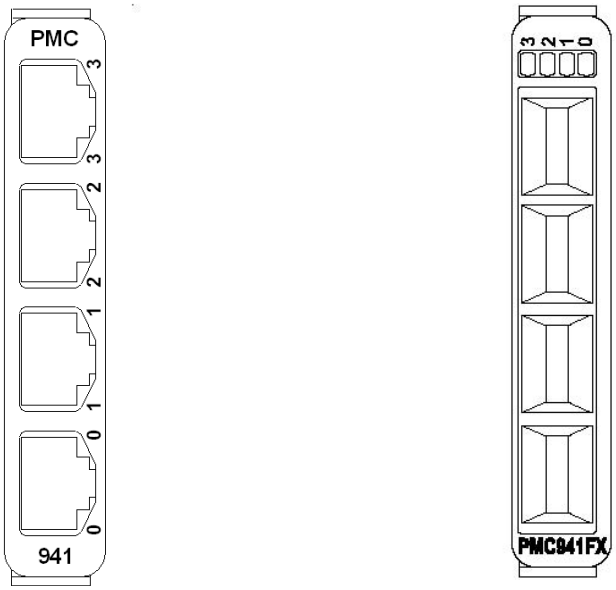
3.2 LED Indicators

There are eight LED's located in the back of the board—one for each of the switch ports.

> ***Note***: There is no indictor for the on-board NIC, since this port is always connected to the switch.

3.3 Link/Activity Indicators

Each port has an associated Link/Activity indicator. The indicator will be illuminated when a valid link is detected. Until a valid link is present, no activity can take place on this port. When packets are received/transmitted on this port, the LINK LED will blink. Thus, if the LED is off, there is no link present. A solid on LED indicates link, but no traffic. A blinking LED indicates that data traffic is on the port.



4 Setting Optional Characteristics

As described in the ***Theory of Operation*** section, the switch fabric can be configured to support QoS, VLAN, and port profile information. This data is captured in an on-card SROM that is loaded into the fabric control engine during power on. The contents of the SROM can be altered on the PMC941/PMC941FX using a special utility running on the Host OS.

Note: If needed, contact GE Fanuc Embedded Systems to receive a copy of the programming tool. There is no charge for this program. This program may not exist on every OS.

SROM contents may also be set at the factory. Consult your GE Fanuc Embedded Systems sales representative for information on this service.

5 I/O Pin Assignments

The PMC941/PMC941FX uses the user-assigned pins of the J4 to route four of its 10/100BaseTX interfaces to the rear. Each of the eight ports has six signals. Only four of the signals are essential; the remaining two signals are common mode outputs from the isolation transformer (these signals are optional).

To connect to a standard UTP cable (RJ45), only the Tx and Rx signal pairs could be used.

Port	Tx +	Tx -	Rx +	Rx -	Shield	CTX	CRX
4	26	25	29	30	32	27	28
5	21	22	18	17	24	19	20
6	10	9	13	14	16	11	12
7	5	6	2	1	8	3	4

6 Software Support

GE Fanuc Embedded Systems has software drivers for all popular operating systems (e.g., VxWorks, HPUX, Solaris, LynxOS, Digital UNIX). These drivers have been carefully designed and implemented to fit within the LAN protocol stack of the host operating system. Thus, all facilities available from the host OS can be utilized across the PMC941/PMC941FX. Customers can change the factory default port setting. GE Fanuc Embedded Systems provides tools to change these parameters under each OS. Consult with GE Fanuc Embedded Systems on the availability of the OS tool.

7 Specifications

Part number	PMC941/PMC941FX	
Software Environment	(SEV) VxWorks	(SED) Digital UNIX
	(SEL) LynxOS	(SES) Solaris
	(SEP) pSOS	(SEH) HPUX
	(SET) NT 4.x	(SEU) Custom
Processor Architecture	(ARC) Power PC	(AR6) R6000
	(AR8) 68K	(ARF) ALPHA
	(ARS) SPARC	(ARA) PA-RISC
	(ARP) x86	(ARX) Custom
Example	PMC941-SEV-ARC: PMC941 in VxWorks environment on Power PC	

7.1 Functional Specifications

I/O Connections	Flush Mounted RJ45
Compatibility	PCI REV. 2.1 IEEE 1386 (PMC) IEEE 802.3 ANSI 8802-3 100BaseTX/10BaseT

7.2 Operating Systems

Drivers	VxWorks, pSOS, Lynx, Digital64, HP-UX, Linux, Solaris, NT

7.3 Electrical / Mechanical

Power	+5V. 4 Watt MAX
Size	IEEE 1386, Standard Single PMC Card
Ports	4 ports routed to the J4 connector
Connectors	J1, J2 and J4
Temperature	Operating 0° C to +65° C Storage -40° C to + 85° C
Relative Humidity	5% to 95% (non-condensing)

GE Fanuc Embedded Systems Information Centers

Americas:
1-800-GE FANUC or (256) 880-0444

Asia Pacific:
86 (10) 6561 1561

Europe, Middle East and Africa:
33 (0)1 4324 6007

Additional Resources

For more information, please visit the
GE Fanuc Embedded Systems web site at:
www.gefanuc.com/embedded