

Hardware Reference Manual

PMC421 Intelligent Serial, 8-Port

DDC No. Rx-URMH 002 Rev -Issued 12 November 2002

it's all about connexions

This page intentionally left blank.



Notice

The information contained in this manual has been carefully reviewed and is believed to be entirely accurate. However, RAMiX shall not be liable for errors contained herein.

Users are encouraged to recommend improvements for future revisions.

RAMiX reserves all rights to make changes to improve reliability, function or design without notice.

Customer Support

To obtain quick technical support, use our email hot-link: <u>support.embeddedsystems@gefanuc.com</u>.

Corporate Headquarters

RAMiX Inc. 1672 Donlon Street, Ventura, CA 93003, USA Tel: 1+805-650-2111 • Fax: 1+805-650-2110 http://www.gefanuc.com/embedded

RAMiX Europe Ltd. 3/2 Great Michael House, 14 Links Place Edinburgh EH6 7EZ, United Kingdom

Tel: +44 131 561-3520 • Fax: +44 131 561-3521

©Copyright 2005 RAMiX Inc. All rights reserved. No part of this document may be reproduced, by any means, without the prior written consent of the copyright holder. Reproduction without written consent constitutes infringement under the Copyright Law of the United States.



1 Introduction

This document describes the operation, design and use of PMC421 Serial Input/Output (I/O) card. With a design combining available embedded processor technology, and high-density serial components, the PMC421 offers a distinct advantage over traditional serial I/O cards. The result is a solution suitable for a wide range of applications, from low speed character I/O to demanding multi channel protocol engines.

1.1 Features

The PMC421 is a powerful and flexible solution to integrate serial data channels to a PCI system. Features include:

1.1.1 PMC421

- PMC Form Factor
- On-Board CPU to Off-Load Host
- Character Blocking & direct memory access (DMA) for Efficient PCI Utilization
- Baud Rate from 150bps 1.5Mbps
- Software Selectable RS232, RS422, RS485 (Full Duplex & Half Duplex)
- All Ports Fully Independent
- Custom Firmware Options for Special Purpose Applications

The PMC421 provides a uniquely effective solution for integrating serial I/O requirements into a VMEbus or CompactPCI system. Implemented on a single PMC card, the PMC421 is fully compatible with current generation VMEbus and CPCI Single Board Computers, as well as any special purpose processor that includes a PMC connector. In addition, card edge PCI systems can be accommodated using RAMiX's PMC239 adapter for rapid prototype and development.

Traditional single and multi-port Serial Interfaces place a high overhead on the host processor by requiring percharacter-attention (i.e., each received and transmitted character generates interrupts and programmed I/O from the host). Two features of the PMC421 remove this overhead:

- On-card CPU for character blocking/unblocking
- Deep FIFO buffers to avoid data overrun (128 Bytes on each port) plus 4MB

Direct control of the 8 Serial Ports (UART) is provided by the on-board processor, a 32-bit RISC CPU. This processor includes DMA engines for efficient transfers over the PCI (over 100Mbytes/second). Data is buffered in the on-card DRAM between transfer to/from the UART interface. In addition to off-loading basic character manipulation, special data handling routines can readily be added to the local processor. Examples include encryption/description, special protocol handling, error correction, etc.

The PMC421 also provides several unique Serial I/O features. Each port has individually programmable line drivers to set any of the most popular signaling types: RS232, RS422 and RS485 (full duplex & half duplex). The



signaling characteristics are software controlled on a per-port-basis. The baud rate of each serial port is also separately programmable: supported rates are from 150bps to 1.5Mbps.

Each port may use simple 3wire connection (TX/RX/GND) or full modem control. Hardware (RTS/CTS), Software (Xon/Xoff) or no flow control is also set per-port via software. The PMC421 can be viewed as four functional components:

1.1.2 PCI Interface

The PMC421 PCI interface is Revision 2.1 compatible, supporting 33MHz/32bit transactions. Both slave and master operation are available, the latter including DMA engines capable of long PCI bursts. As data is buffered in local DRAM, large blocking factors can be used (when application level protocols allow). Both programmed I/O and message-based control is supported. The messaging system follows I2O hardware specifications.

1.1.3 Processor Resources

The on board 32 bit RISC CPU (i960VH) provides an external bus rate of 33MHz and an internal processor clock rate of 100MHz. The higher CPU clock rate ensures sufficient bandwidth for all protocols (e.g. encryption) and character manipulation at high, multi-port data rates. Local DRAM (4 Mbytes) is used for firmware execution and character data buffering. Firmware is loaded automatically on power-up from local FLASH memory. New firmware (e.g., upgrades) may be loaded in the field without removing the PMC421 from the host. The processor directly controls both the UARTs and the Signal Drivers for full software configuration.

1.1.4 Programming Interface

Flexibility, efficiency and use with both new and existing applications were all considered during the design of the Application Interface. Several modes of data transfer are supported, including a traditional programmed I/O (i.e., pseudo register) and high performance messaging. The "pseudo register" interface allows a host to use programmed I/O cycles to set characteristics and transmit/receive data. While less efficient, this mode can be appropriate for simple (low-speed) operation as well as when adapting legacy code. The messaging interface allows simple, efficient transfers between host software and the PMC421. A control block contains transaction-specific information such as configuration, data or location of data buffers. A message queuing system makes transfer of the control blocks between the host and PMC421 very simple with minimal software development. Once submitted to the PMC421, the transaction information is loaded by the local processor; for large data blocks, the DMA engines are utilized to execute the data movement. This improves PCI bus utilization as well as allowing scatter/gather operation (useful in virtual memory operating systems).

1.1.5 Serial Ports

Each serial data stream is controlled with a UART, which is responsible for Serialization/De-Serialization and, if enabled, hardware flow control. Each serial port has independent configuration parameters for speed and flow control, etc. Intrinsic to each UART is a deep FIFO buffer to prevent data loss under high or bursty loads. The UART can also control software flow control, ensuring very rapid response to the incoming data stream.

1.1.6 Line Drivers

In traditional Serial Interface cards, the various electrical signaling protocols (e.g., RS232, RS422) were configured via switches or jumpers. This increases the potential for difficult-to-detect-errors. On the PMC421,



each serial interface has a line driver that is configured and controlled directly from the local processor, enabling each line to be set to the application requirement via software control.

1.1.7 External Connection

The PMC421 offers both front and rear I/O. The front I/O is a high-density 68-pin connector. The 68-pin connector mates with a separate cable to provide standard connection to 8 DB-9 male connectors (purchased separately). For applications that require rear I/O, the ports are wired to the J4 connector of the PMC421.



2 Theory of Operation

Handling serial I/O data generally imposes a high overhead on a processor. Data is converted to/ from a serial bit stream by a UART device, which is character-based, usually with none to low amounts of internal data storage. As a result, there is a distinct time constraint on the host to feed the UART. Failure to unload data will result in data overrun (and lost information), not keeping the output filled reduces total data rate.

Modern processors and I/O bus protocols (e.g., PCI) are particularly unsuited for character style I/ O. Processor performance is predicated on maintaining a continuous pipeline of data and instructions; interactions with external I/O devices break the smooth flow of processing. I/O buses (such as PCI) extend this design in their realm, depending upon longer burst (i.e., multiple cycle) transactions to mitigate protocol overheats. Single cycle (e.g., one to four byte) transactions on the PCI will be an order of magnitude less effective than burst transactions. Each I/O device that requires fine grain control decreases the overall system performance by consuming an excessive proportion of total resources.

While there are some UART devices with DMA capabilities, these are of limited use; setup overhead reduces effectivity for small transfer sizes. In addition, serial data streams frequently include low-level protocols that demand per-character response. (A simple example is software flow control.)

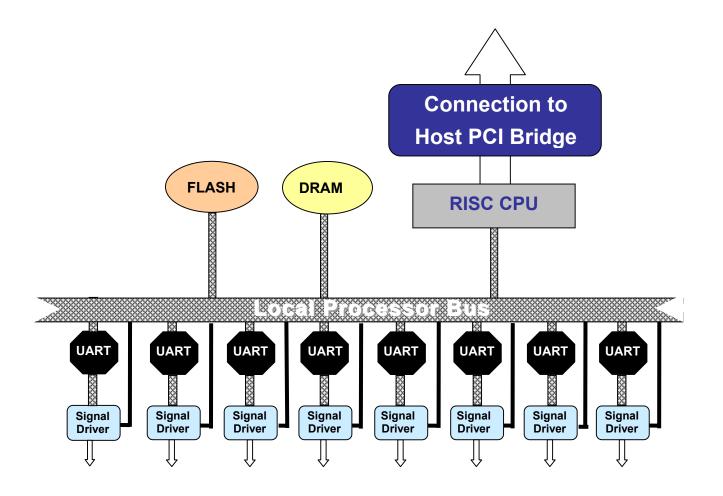
Inserting a processor into the design results in several benefits:

- Decoupling connection to UART and host
- Flexible engine to multiplex/demultiplex application buffers to/from UARTs
- Dedicated resource to handle UART control to keep all channels operating at full line speeds
- Provision to augment firmware with special protocol handling (e.g., encryption) with minimum effort. (All firmware is in high-level language.)

The PMC421 takes advantage of the most recent technology in UART implementation, which allows deeper hardware buffers and control to further augment overall data flow.

Refer to the block diagram for the design of the PMC421.





2.1 Functional Components

The PMC421 can be broken into several functional components:

- PCI Interface
- intelligent Co-Processor (IOCP) Firmware execution
- UART (Data serializes)
- Signaling Drivers

The following paragraphs describe each component.



2.1.1 PCI Interface

The PMC421 PCI interface is compliant with revision 2.1 of the specification. It supports up to 33MHz operation with 32-bit data path. Functions within the interface that augment the operation of the PMC421 include:

- DMA engines to move larger data packets efficiently over the bus
- Message passing hardware supporting simple and efficient application API

2.1.2 IOCP

The IOCP (Intelligent Co-processor) refers to the local CPU, which executes the PMC421 firmware. It is a full function, 32-bit RISC processor. The firmware is based upon the open source Real Time Operating System (RTOS) RTEMS which was developed by the US Army. It provides all functionality expected from an embedded kernel, and strongly enhances the modularity of the RAMiX firmware design. The basic firmware handles off-standard functions (e.g., UART configuration, block and character oriented data transfer, etc.).

Initial configuration is extremely simple, as is operational use. This is a result of having all detailed control of the UART performed by the firmware library. In most software device drivers, a substantial component (and usually much of the complexity) is in device-specific setup. All of this is performed by easily invoked library functions.

The firmware uses the DMA engines whenever possible to maximize PCI efficiency. Again, the benefit of using the dedicated IOCP is apparent. DMA engine setup is not required by the host, as the IOCP will master all data movement.

2.1.3 UART

The UART components chosen for the PMC421 are recent implementations that provide enhanced features and small package size. Features include deep FIFO hardware buffers for each port (128 Bytes per port) as well as a number of on-chip capabilities to maintain full wire speed while minimizing timing constraints on the IOCP. Each port is configured independently for baud rate and flow control options. Full modem or three wire operation can be selected on a "per port" basis.

2.1.4 Signaling Drivers

A design goal of the PMC421 was to maximize the amount of configuration that can be done under software control, including setting of the electrical signaling characteristics. Each port can be set to RS232, RS422 or RS485 signaling standard under software control of the IOCP.



3 Handling And Installation

3.1 Handling Precautions

Electronic assemblies use devices that are sensitive to static discharge. Observe anti-static procedures when handling these boards. All products should be in an anti-static plastic bag or conductive foam for storage or shipment. Work at an approved anti-static work station when unpacking boards.

3.2 Unpacking Instructions

RAMiX products are shipped in individual, reusable shipping boxes. When receiving the shipping container, inspect it for any evidence of physical damage. IF the container is damaged, request that the carrier's agent be present during the unpacking of individual boxes and the inspection of each unit.

Remove the PMC module from the shipping box and anti-static packaging. Verify that it is not damaged and that all items are present by referring to the packing list.

3.3 Installation

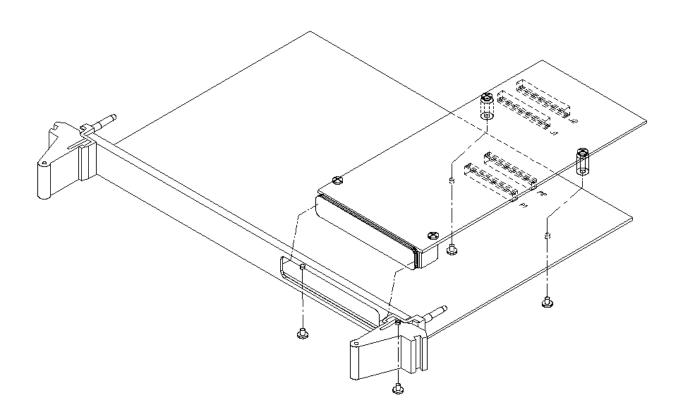
The PMCModule is now ready for installation. Installation is done generically as with the commercial versions of the card. Follow any specific procedures recommended by the manufacturer for the chassis used.

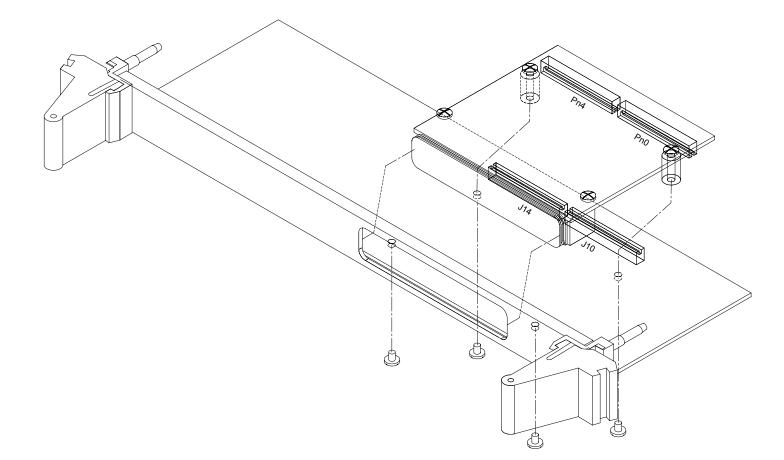
Turn all system power OFF. Remove the host board from the chassis (if currently installed). Locate the PMC connectors on the host board. Carefully plug the PMC into the mating connectors on the host's Printed Circuit Board (PCB). Be sure the PMC module is seated properly into CMC connectors on the host. Refer to the following pages.



Use screws to fasten module into host PCB.

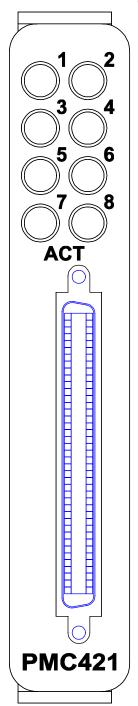
- Remove the four screws from bottom of the stand-offs of the PMC.
- Line-up the J1 and J2 connectors on the host CMC to the J1 and J2 connectors on the PMC card.
- Ensure all connectors are properly aligned before pushing the connectors together.
- Use the four screws to connect the PMC stand-offs to the host CMC.







4 Front Panel Connections And Indicators



PMC421

Each serial port has a related activity LED.



4.1 I/O Signal Pin-outs

Each serial port has four control signals:

- TX Transmitted Data
- RX Received Data
- CTS Clear To Send (Receive FIFO not full)
- RTS Ready To Send (TX FIFO not empty)

To support differential signaling standards (e.g., RS422), each signal has a positive and negative line. When using a single ended standard (e.g., RS232), use the negative version. All I/O signals are available both at the front panel connector and on the J4 "backplane" connector. The following table details all connections:

Port	Signal	Front Panel Pin		J4 Pin	J4 Pin	
		Positive	Negative	Positive	Negative	
1	RX	2	1	2	1	
	ΤX	4	3	4	3	
1	RTS	6	5	6	5	
	CTS	8	7	8	7	
2	RX	36	35	10	9	
	ΤX	38	37	12	11	
2	RTS	40	39	14	13	
	CTS	42	41	16	15	
	RX	11	10	18	17	
3	TX	13	12	20	19	
3	RTS	15	14	22	21	
	CTS	17	16	24	23	
	RX	45	44	26	25	
4	ТΧ	47	46	28	27	
-	RTS	49	48	30	29	
	CTS	51	50	32	31	
	RX	19	18	34	33	
5	ΤX	21	20	36	35	
5	RTS	23	22	38	37	
	CTS	25	24	40	39	
	RX	53	52	42	41	
6	ТΧ	55	54	44	43	
0	RTS	57	56	46	45	
	CTS	59	58	48	47	
	RX	28	26	50	49	
7	TX	30	29	52	51	
1	RTS	32	31	54	53	
	CTS	34	33	56	55	
8	RX	62	60	58	57	
	ТΧ	64	63	60	59	
	RTS	66	65	62	61	
	CTS	68	67	64	63	



Ground is available on the front panel connector on pins 9, 27, 43 and 61.

4.2 Front Panel Connector

The front panel connector is a high density SCSI Female connector, AMP part number AMP-796055-1.

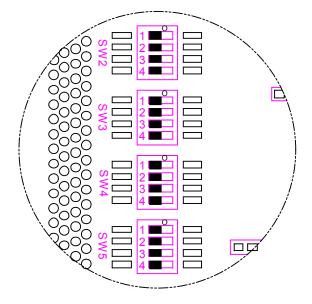
4.3 DIP Switches

4.3.1 RS485 Support (SW2-SW5)

These switches are used when running a port in RS485 signaling mode. When running RS485, the two switches associated with the port should be **Closed**. In all other signaling modes, the switches should be **Open** (see the table below for port/switch position assignments).

<u>Note</u>: The use of RS485 requires use of the correct software interface. Consult the driver manual for the operating system used for details.

All switches are in the **Open** state when shipped from the factory.

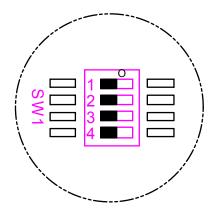


Switch Pack	Switch Number	Port
SW2	1	0
SW2	2	0
SW2	3	1
SW2	4	1
SW3	1	2
SW3	2	2
SW3	3	3
SW3	4	3
SW4	1	4
SW4	2	4
SW4	3	5
SW4	4	5
SW5	1	6
SW5	2	6
SW5	3	7
SW5	4	7



4.3.2 Processor Control (SW1)

SW1 controls the initialization status of the on-card processor. It should not be altered from factory default. Any change will prevent correct operation of the PMC421 firmware. Factory Default setting is:



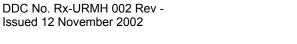
SW1 Switch Pack		
Switch Number	Position	
1	Open	
2	Open	
3	Open	
4	Open	



5 Functional Specifications

5.1 PMC421

4 Total Watts
0.6 Amp
Single Slot
218000 Hours
0 to +60° C
-40 to +85° C
5% to 95% Non-Condensing
5% to 95% Non-Condensing
Yes, additional charge
3 & 5V
2.2
2.2 33MHz
32
32
32
32
8
8
8 (8) Serial ports via 68 pin SCSI





5.2 PIM422

PIM422 PIM Transition Module for PMC421, PMC422 or PMC423

Power	0 Total Watts	
MTBF		
MIL 217-F Nav Shel 25 Deg. C	600000 Hours	
Temperature		
Operating	0 to +60° C	
Storage	-40 to +85° C	
Humidity		
Operating	5% to 95% Non-Condensing	
Storage	5% to 95% Non-Condensing	



Corporate Headquarters RAMiX Inc 1672 Donlon Street, Ventura, CA 93003, USA

Tel: 1+805-650-2111 • Fax: 1+805-650-2110

RAMiX Europe Limited 3/2 Great Michael House, 14 Links Place Edinburgh EH6 7EZ, United Kingdom

Tel: +44 131 561-3520 • Fax: +44 131 561-3521