

CR5

3U Rugged Intel® Core™ 2 Duo LV Processor CompactPCI® SBC

Features

- Intel® Core™ 2 Duo LV processor @ 1.5 GHz with 4 Mbyte L2 cache
- Intel Core Duo LV processor @ 1.66 GHz with 2 Mbyte L2 cache
- Intel 3100 Integrated Memory and I/O Controller Hub (MICH)
- Up to 1 Gbyte DDR2 SDRAM with ECC on 400 MHz memory bus
- CompactFlash module on mezzanine board
- 2x Gigabit Ethernet
- 1/2x external SATA ports
- 2x USB 2.0 ports
- 2x COM ports
- 8x GPIO ports
- System controller or peripheral operation
- Convection- and conduction-cooled configurations
- Extended temperature range (-40° to 85° C)
- Operating system support for VxWorks®, Linux®, and Windows® XP
- Contact the factory and/or the product manual for temperature ranges for specific CPUs
- RoHS compliant

CR5 is the next generation of rugged 3U CompactPCI Single Board Computers offering an Intel Core 2 Duo LV processor that features 65 nm technology with a core processing speed up to 1.5 GHz. This Intel processor delivers two complete execution cores that share a 667 MHz front-side bus (FSB) and 4 Mbyte of L2 cache in one processor package.

The 3100 MICH supports 1-lane and 4-lane PCI-express Interfaces, two USB 2.0 ports, two COM ports, and one internal and two external serial ATA ports. The CR5 also features a custom mezzanine board providing CompactFlash and SVGA.

For general status and control capability, the CR5 provides eight programmable General-purpose I/O (GPIO) lines with separate Interrupts and Interrupt masking.

The CR5 is available in convection- and conduction-cooled configurations.

Specifications

Processor

- Intel Core 2 Duo LV Processor with core processor speed of 1.5 GHz
- Intel Core Duo LV Processor with core processor speed of 1.66 GHz
- Two complete execution cores in one processor package
- High performance, low power, Intel Dual Core Architecture
- 4 Mbyte L2 on-chip cache (Intel Core 2 Duo processor)
- 2 Mbyte L2 on-chip cache (Intel Core Duo processor)
- 667 MHz front side bus

Memory – SDRAM

- Up to 1 Gbyte DDR2 SDRAM with ECC
- Integrated DDR2 SDRAM Controller through 3100
- 400 MHz Memory Bus (72-bit)

Flash ROM

- 1 Mbyte BIOS array
- Multiple levels of write-protection

CompactFlash

- Up to 8 Gbyte
- Single Type I CompactFlash module on an UltraDMA 100 IDE bus interface via a SATA bridge
- CompactFlash connector is located on the mezzanine board

Serial ATA

- Dual external SATA support via the 3100 MICH
 - SATA0 to rear J2
 - SATA1 to rear J2 (requires build option that drops synchronous clocks on COM2 and matching CR5-TM)

CPCI Backplane Bridge info

- PLX6254 cPCI interface
- 32-bit/33 MHz cPCI data transfers
- * System controller or peripheral slot operation
- * VIO = +5V or +3.3V

Ethernet

- Intel 82571EB provides dual Gigabit Ethernet with integrated MAC and PHY routed to J2

Video

- Mezzanine required for video controller
- SVGA: 640x480 to 1600 x 1200 (UXGA) pixel field, 32 bits/pixel

Real Time Clock

- Integrated real-time clock through the 3100 MICH
- Battery backup from system



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Counters/Timers

- Three programmable timers provided via Intel 3100 MICH
- Timer 0 is system timer and configurable as 32 or 64 bits wide
- Timer 1 provides the memory refresh request signal and is 32 bits only
- Timer 2 is used for speaker tone and is 32 bits only
- Three additional High-Precision Event Timers (HPETs) for use by the operating system
- HPET 0 is configurable as either a 64-bit or a 32-bit timer
- HPET 1 and 2 are 32-bit only timers

Temperature Sensor

- CPU die and ambient temperature
- Software readable -55° to +125° C

Serial Ports

- COM1: RS-232, routed to J2
- COM2: RS-422/485, routed to J2, asynchronous or synchronous

USB I/O

- Dual USB 2.0 ports routed to J2
- Integrated USB controller through the 3100 MICH

GPIO

- FPGA GPIO Controller
- Eight general-purpose I/O lines to backplane
- Configurable interrupt and individual interrupt masking

Power Requirements

- +5 V, +3.3V
- +3.3V (required on cPCI_J2 VBATT for RTC battery backup)

Power Consumption

	+5V	+3.3V
• Peak:**	7.8A	6.6A
• Max. sustained:**	5.7A	5.9A
• Idle:**	TBD	TBD
• Inrush:	TBD	TBD
• VBATT:	TBD	TBD
• Total:	TBD	TBD

*Calculated values
**Measured at DOS prompt

Temperature

	Operating	Storage
• Convection*	0° to +70° C	-40° to +85° C
• Conduction**	-40° to +85° C	-55° to +105° C

*Minimum airflow of 400 LFM required

**Measured at card edge

Contact the factory for temperature ranges for specific CPUs and variants

Mechanical

- PICMG 2.0 and VITA 30.1 compliant
- 3U, 1 slot wide
- 100 mm x 160 mm x 20 mm
- Weight: Convection TBD
Conduction TBD

Humidity (non-condensing)

- Operating: 5-95% @ 40° C*
- Storage: 5-95% @ 40° C*

Altitude: TBD

Shock: TBD

Vibration: TBD

MTBF

- Calculations are available in accordance with MIL-HDBK-217. Please contact GE Fanuc for latest values.

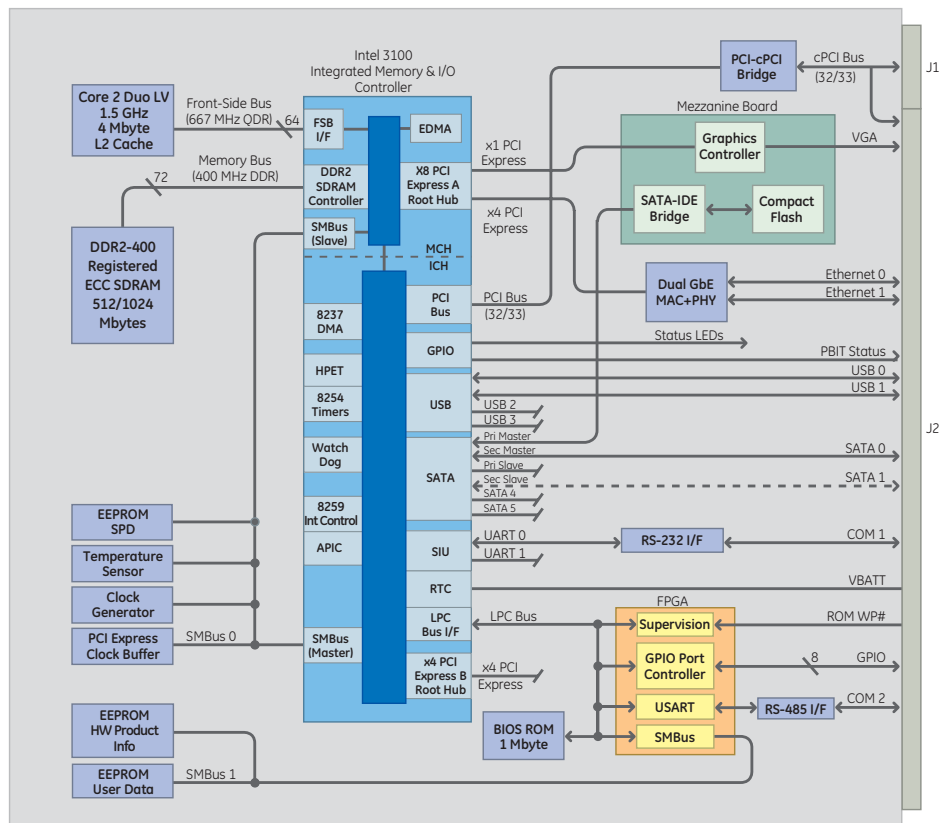
Safety

- Designed to meet standard UL1950/60950

Emissions

- Designed to meet FCC Part15, SubPart A

Block Diagram



Ordering Information

- CR5321X01:** Intel Core 2 Duo LV @ 1.5 GHz, 1 GB DDR2 SDRAM, RoHS, convection cooled
- CR5221X01:** Intel Core Duo LV @ 1.66 GHz, 1 GB DDR2 SDRAM, RoHS, convection cooled
- CR5221X08:** Intel Core Duo LV @ 1.66 GHz, 1 GB DDR2 SDRAM, RoHS, conduction cooled

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Additional Resources

For more information, please visit the GE Fanuc Intelligent Platforms web site at:

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