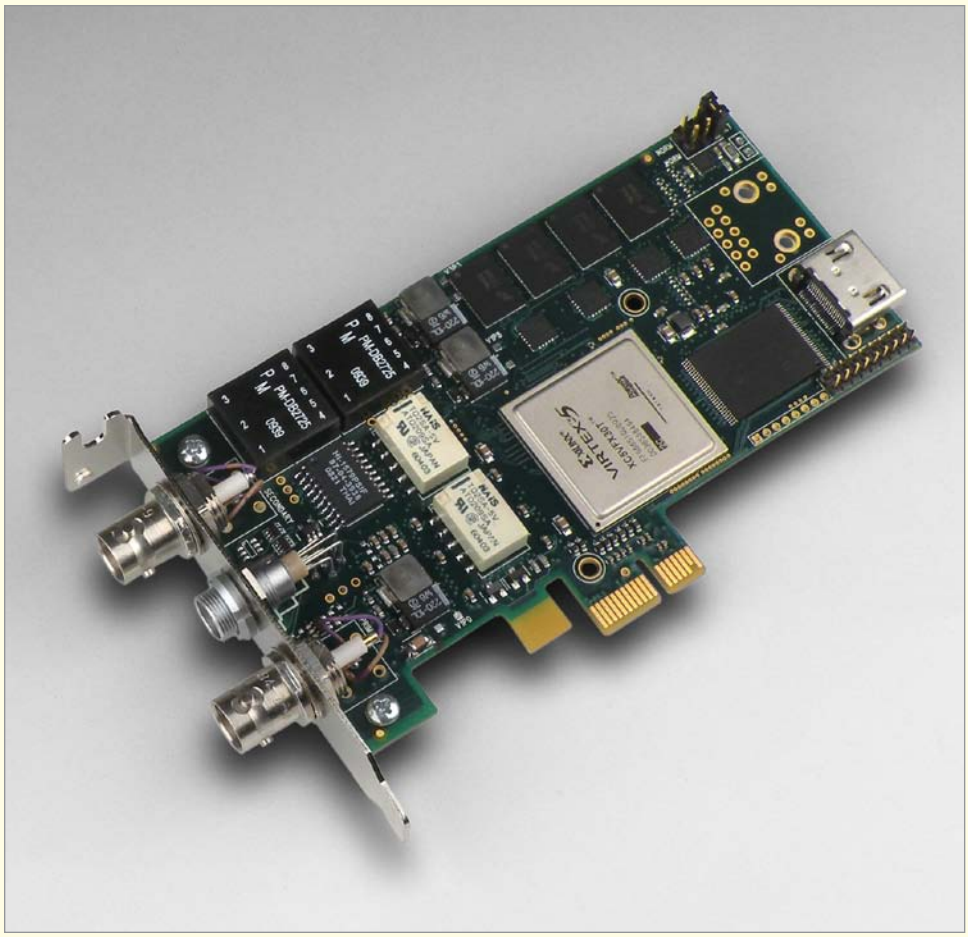
PCIe1 53B

PCI Express x1 interface for MIL-STD 1553B



Features

- PCI Express x1 interface (80 MB/s) for 1553B with full- or half-height backpanel
- Supplies a bus controller, a bus monitor, and thirty-one remote terminals (RTs), all running concurrently and independently
- Provides one Xilinx Virtex 5 FPGA (XC5VFX30T) with an embedded processor (PowerPC 440) that includes local memory
- Has dual-redundant 1553B bus interface, serial debug interface, and IRIG-B time code input
- Supports minimum 4-microsecond intermessage gap for RT response
- Allows real-time scheduling and error insertion / deletion
- Supports direct or transformer coupling to 1553B bus
- Provides extensive built-in test facility
- Supports backwards compatibility with PCI 53B software
- Can be configured by user to work with any 1553A or 1553B protocol, or to detect any standard command or subcommand as illegal

Description

PCIe1 53B is a PCI Express one-lane interface (80 MB/s) for MIL-STD 1553B with a full-height or half-height backpanel. The board supplies one bus controller, one bus monitor, and thirty-one remote terminals (RTs); all run concurrently and independently. Also provided onboard is one EDT-programmable Xilinx Virtex 5 FPGA, which includes an embedded processor (PowerPC 440) with local memory.

The board features a dual-redundant 1553B bus interface, serial debug interface, and IRIG-B time code input. It supports the minimum 4-microsecond intermessage gap for RT response; powerful capabilities for real-time scheduling and error insertion / detection; direct or transformer coupling to the 1553B bus; and all mode codes for dual redundant operation. It also has an extensive built-in test facility and is compatible with PCI 53B software.

The board is programmable for multiple 1553 protocols (A or B by user, others by EDT). The board supports the full 1553B standard, but can be configured to detect any standard command or subcommand as illegal.

After initialization, the application program can configure the board as required. EDT provides FPGA configuration files, drivers for supported operating systems, and a software development kit that includes C language libraries, examples, and utilities.

Applications

MIL-STD 1553B communications

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Specifications

Product Type	PCIe1 53B-LP is a 1-lane PCI Express interface for MIL-STD 1553B; it provides DMA, memory, embedded processor, and FPGA resources.	
FPGA & Processing Resources	One EDT-programmable FPGA One embedded processor (in FPGA)	Xilinx Virtex 5 (XC5VFX30T) PowerPC 440
Other Resources	One bus monitor One bus controller Thirty-one remote terminals (RTs) User-programmable register to select direct or transformer coupling to 1553B bus	
Memory (on Processor)	SRAM DRAM Flash ROM	8 MB 512 MB 8 MB
Interfaces	PCIe bus MIL-STD 1553B bus Serial debug Time code input	One; data rate = 80 MB/s One (dual-redundant, all mode codes supported); data rate = full bus bandwidth One One (IRIG-B)
PCI Express Compliance	PCIe version Direct memory access (DMA) Number of lanes	1.1 Yes One (80 MB/sec)
1553B Compliance	Fully compliant	
Backpanel	Full-height or half-height	
Connectors	MIL-STD 1553B Serial debug & time code input (IRIG-B)	Two King 1994-1-9 Triax Lemo 7-pin
Cabling	Cabling is purchased separately; consult EDT for options.	
Physical	Weight Dimensions	2.8 oz. typical 4.75 x 2.75 x 0.5"
Environmental	Temperature Humidity	Operating 10° to 40° C Non-operating -20° to 60° C Operating 20% to 80%, non-condensing at 40° C Non-operating 95%, non-condensing at 40° C
System and Software	System must have a PCI Express bus (1 to 16 lanes). Software is included for Windows and Linux; for versions, see our website.	

Ordering Options

Backpanel: **Full height** / half height

Bold is default. **Ask about custom options.**