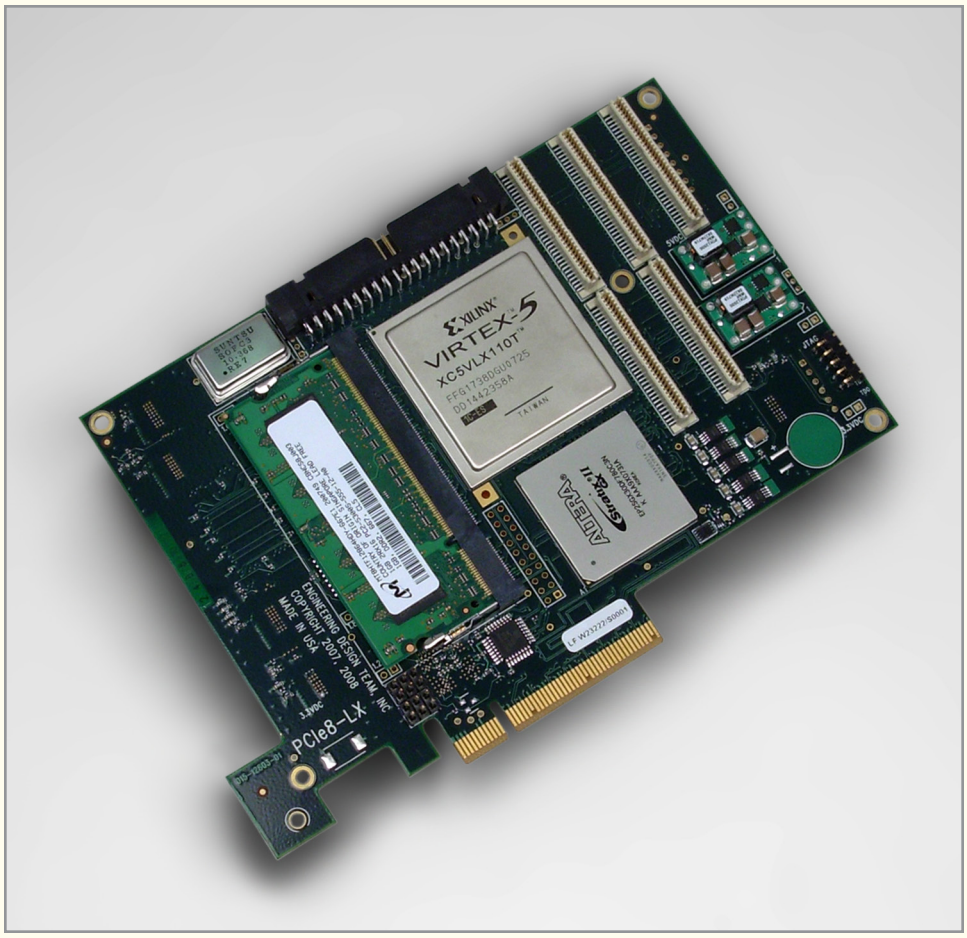
edt
a HEICO company

PCIe8 LX / FX / SX

PCI Express 8-lane DMA interface with multiple FPGA options



Features

- Main board (for an 8- or 16-lane PCIe slot) – provides an EDT mezzanine board with DMA, programmable FPGA resources, and memory
- Alternatively, can be used as an accelerator board (with no mezzanine board)
- 221 LVTTL programmable signals connected to mezzanine board (if used)
- FPGA: One programmable Xilinx Virtex 5 (LX / FX / SX) + connectors as below.
  - LX: XC5VLX110T (or optional 220T or 330T) + QSH or optional ATA
  - FX: XC5VFX100T (or optional 130T) with two PowerPC 440 processors + QSH
  - SX: XC5VSX240T + QSH
- SRAM: 8 MB
- DRAM (DDR2): 0 or optional 1 GB or 2 GB
- Clocks: Four independent programmable PLL clock generators

Description

The PCIe8 LX / FX / SX is a PCI Express (PCIe) 8-lane interface that can be used as a main board to provide resources to a mezzanine board, or used alone as an accelerator (FPGA board). It works in an 8- or 16-lane slot.

The board has one user-configurable Xilinx Virtex 5 FPGA, which can be LX (XC5VLX110T or optional 220T or 330T), FX (XC5VFX100T or optional 130T), or SX (XC5VSX240T). The LX has an 80-pin QSH or optional 40-pin ATA-type expansion connector; the FX and SX have a QSH connector only. The FX includes two PowerPC 440 processors as well.

The board has SRAM of 8 MB and optional DRAM (200-pin SODIMM DDR2) of 1 GB or 2 GB.

There are four independent programmable PLL clock generators, which can be set to select frequencies from 1 to 45 MHz with an error rate of less than +/- 50 ppm.

The board supports virtually any EDT mezzanine board (which provides a fan and a backplane for cooling and mounting), the Time Distribution board and, with the LX ATA option only, an EDT Bridge to link two main boards together.

If the board will be used as an accelerator, it is shipped with an attached fan board and backplane to provide for cooling and mounting.

Applications

- Use as a main board for an EDT mezzanine board
- Use alone as an accelerator (FPGA board)

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Specifications

Product Type	PCIe8 LX / FX / SX is a PCIe x8 board that acts as an accelerator, or supplies DMA, memory, and FPGA resources to a mezzanine board.	
FPGA Resources	One programmable Xilinx Virtex 5: LX (XC5VLX110T or optional 220T or 330T); FX (XC5VFX100T or optional 130T); or SX (XC5VSX240T).	
Memory	SRAM DRAM (200-pin SODIMM DDR2)	8 MB 0 or optional 1 GB or 2 GB
Clocks	Four programmable independent PLL clock generators, each with input and output clocks: Input (reference) clocks can be set to 10.3681 or 40 MHz, or PCIe clock. Output clocks can be set with only +/- 50 ppm error to 1.544, 2.048, 6.312, 8.448, 34.368, or 44.736 MHz.	
Data Rates	Dependent on such factors as data format, mezzanine board, and system variables: Peak Typical	 1.6 GB/s 1.2 GB/s
Data Format (I/O)	Determined by mezzanine board and auxiliaries	
PCI Express Compliance	PCIe version DMA Number of lanes	PCIe 1.1 Up to 16 channels, depending on mezzanine board 8
Connectors	Five CMC-type (IEEE 1386) mezzanine One 6-pin .100" x 1 row square .025" One 8-pin .100" x 1 row square .025" square pins **With LX FPGA:** One standard 40-pin ATA-type expansion Or one optional 80-pin QSH **With FX FPGA:** One standard 80-pin QSH **With SX FPGA:** One standard 80-pin QSH	221 LVTTL I/O (mate to AMP 120527-1 or Molex 71436-2164) For FPGA JTAG (IEEE 1149.1) For six external debugging LEDs 30 LVTTL signals for external board or FPGA debugging 15 LVDS pairs and 4 Xilinx RocketIO RX/TX pairs 15 LVDS pairs and 4 Xilinx RocketIO RX/TX pairs 15 LVDS pairs and 4 Xilinx RocketIO RX/TX pairs
Cabling	Consult EDT for purchase options.	
Physical	Weight Dimensions	3.9 oz. typical 6.6 x 4.2 x 0.75 in.
Environmental	Temperature (operating / non-operating) Humidity (operating / non-operating)	0° to 40° C / -40° to 70° C 1% to 90%, non-condensing at 40° C / 95%, non-condensing at 45° C
System and Software	System must have a PCI Express bus (8 or 16 lanes) that is not dedicated to display use only. Software is included for Windows and Linux, with limited support for Solaris and Mac OS; for versions, see www.edt.com.	

Ordering Options

To use as a main board
- Mezzanine board: See Compatibility Guide.

To use alone, as an accelerator (FPGA board)
- Fan board (with backplane) included

To use as either a main board or an accelerator
- FPGA + connectors:
  - **LX** (XC5VLX**110T** / 220T / 330T) + **QSH** / ATA
  - FX (XC5VFX**100T** / 130T) + QSH only
  - SX (XC5VSX240T + QSH only
- DRAM: **0** / 1 GB / 2 GB

Bold is default. For more options, see mezzanine board detail. **Ask** about custom options.