Net10G

Network processing interface for up to OC192/STM64/10GbE

Description

The Net10G is a mezzanine board that pairs with an EDT main board (for PCI or PCI Express) to support multiple standards. It accepts electrical or optical ethernet of up to 10GbE, and also multiple SONET (SDH) signals.

The Net10G has two high-speed TCAMs and two pluggable form factors: one SFP for OC3/12/48 (STM1/4/16) or 1GbE (electrical or optical); and one XFP for OC192 (STM64) or 10GbE (electrical or optical). It has a programmable FPGA (Xilinx Virtex 5 LX), 2 GB of DRAM, and 8 MB of SRAM. It also has a 1 pps or IRIG-B time code input for precise timestamp data.

EDT provides FPGA configuration files to enable demultiplexing to VC-4C payloads and to support raw, framed, framed and descrambled, header, and payload data. Custom configuration files can be requested.

The main board supplies DMA, plus additional memory and programmable FPGA resources.

Features

- Mezzanine board – pairs with an EDT main board (in a PCI, PCI-X, or PCIe bus), which adds DMA, programmable FPGA resources, and memory
- Channel 0: One optional SFP for 1GbE (electrical or optical) or OC3/12/48 (STM1/4/16), 155.52, 622.08, or 2488.32 Mb/s – 850, 1310, or 1550 nm
- Channel 1: One optional XFP for 10GbE (electrical or optical) or OC192 (STM64), 9953.28 Mb/s – 850, 1310, or 1550 nm
- Encoding: 8b/10b or 64b/66b
- Time code: 1 pps, IRIG-B, or other input, with user-configurable output
- FPGA: One programmable Xilinx Virtex 5 LX XC5VLX110/220/330
- SRAM: 8 MB (2 M x 36) for general use or TCAM-associated data
- DRAM: 2 GB (DDR2) for snapshot recording and data buffering
- TCAMs: Two (with lookup tables, configurable entries, and output tied to FPGA)
- EDT intellectual property for 10GbE media access control layer, SONET/SDH framing, and demultiplexing
- Time code input: 1 pps or IRIG-B (included on the board)

Applications

Multiple network data processing applications

Specifications

Product Type	Net10G is a network processing mezzanine board for up to OC192/STM64/10GbE; it requires a main board.	
FPGA Resources	One programmable FPGA (Xilinx Virtex 5 LX XC5VLX110 or optional 220 or 330), plus FPGA resources on main board	
Memory	SRAM	8 MB (2 M x 36) for general use or TCAM-associated data
	DRAM (DDR2)	2 GB for snapshot recording and data buffering
	TCAMs (with lookup tables and output tied to FPGA)	Two cascading, configurable 40-, 80-, 160-, 320-, or 640-bit entries
Clocks	Programmable internal reference clock with jitter attenuation	
Data Rates	Dependent on such factors as data format, main board, and system variables.	
Data Format (I/O)	Time code (from external receiver)	1 pps, IRIG-B, or other input, with user-configurable output
	Channel 0	1GbE (electrical or optical) or SONET OC3/12/48 (SDH STM1/4/16)
	Channel 1	10GbE (electrical or optical) or SONET OC192 (SDH STM64)
	(Output can be made to meet SONET/SDH jitter specifications if required.)	
Protocols	SONET/SDH - STM1/4/16/64 - concatenated payload; other payloads available upon request Ethernet - IEEE802.3, packet over SONET; header-only or header and payload available upon request	
Transceivers	One optional SFP and one optional XFP are available, supporting the data formats shown below.	

CHANNEL 0	**Electrical: 1GbE**	**Optical: 1GbE or OC3/12/48 (STM1/4/16)**		
(SFP)	**(1000 Base-T)**	**850 nm**	**1310 nm**	**1550 nm**
Output power	–	-9 to -2.5 dBm	-9.5 to -3 dBm	-2 to 3 dBm
Center wavelength	–	830 to 860 nm	1270 to 1360 nm	1500 to 1580 nm
Sensitivity	–	-18 dBm	-18 dBm	-28 dBm
Maximum input power	–	0 dBm	0 dBm	-9 dBm
Connector	RJ45	LC	LC	LC

CHANNEL 1	**Electrical: 10GbE**	**Optical: 10GbE or OC192 (STM64)**		
(XFP)	**(10G Base-CX4)**	**850 nm**	**1310 nm**	**1550 nm**
Output power	–	-3 to -1 dBm	-6 to -1 dBm	-1 to 2 dBm
Center wavelength	–	850 nm	1290 to 1330 nm	1550 nm
Sensitivity	–	-7.5 dBm	-13 dBm	-15 dBm
Maximum input power	–	-1 dBm	-0.5 dBm	-1 dBm
Connector	CX4	LC	LC	LC

Connectors	One 7-pin Lemo for time code input One RJ45, LC, or CX4 on each transceiver as shown above	
Cabling	Consult EDT for purchase options:	
	To 7-pin Lemo on board, from time code source	Via one DB9 (for 1 pps or IRIG-B) or BNC (for IRIG-B only)
Physical	Weight	7.7 oz. typical
	Dimensions	6.6 x 4.2 x 0.5 in. (with a main board)
Environmental	Temperature	Operating 0° to 40° C Non-operating -40° to 70° C
	Humidity	Operating 1% to 90%, non-condensing at 40° C Non-operating 95%, non-condensing at 45° C
System and Software	For details on system requirements and EDT-provided software driver packages, see specifications for your EDT main board.	

Support

EDT offers engineer-to-engineer customer support, from phone consultation to custom design of hardware, firmware, and software. Contact us for options and details.

Contact

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Ordering Options

- Main board: PCI GS / PCIe8 LX
- FPGA: XC5VLX**110** / 220 / 330
- Transceivers: 1 SFP and 1 XFP (options above)
- Cabling: DB9 / BNC

Bold is default. For more options, see main board detail. **Ask** about custom options.