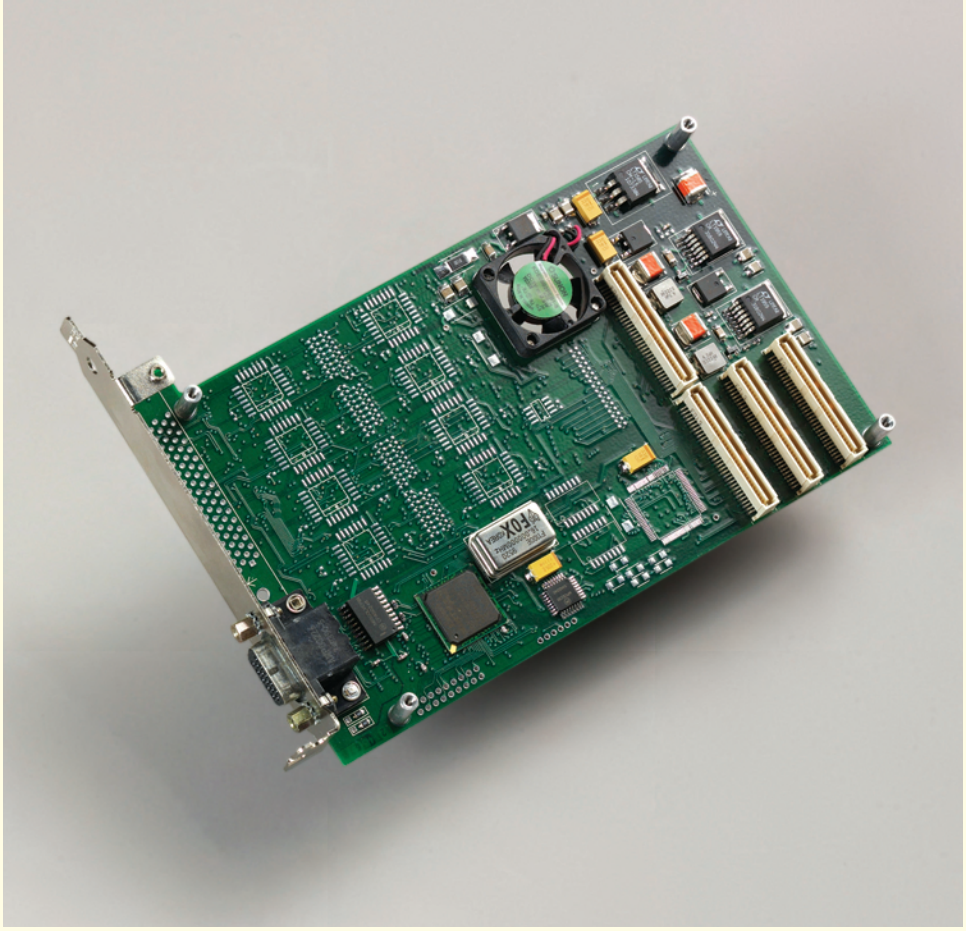
edt
a HEICO company

SSE

Synchronous serial ECL interface



Description

The SSE is a mezzanine board that pairs with an EDT main board (for PCI or PCI Express) for high-speed data transfer. It supports three channels (two input and one output) of ECL.

The SSE samples the data on the rising edge of the clock and stores it in host memory via the main board. Each channel supports one differential data signal (two wires) and one differential clock (two more wires). Input signals are terminated through 50 Ω to -2 V.

The SSE can be custom-configured to support thirty-two additional ECL, LVDS, or RS422 signals in groups of four. The board also can be configured to support one additional signal for applications requiring notification of the start or end of a block transfer. For details, contact EDT.

The main board supplies high-speed DMA, plus additional memory and programmable FPGA resources.

Features

- Mezzanine board – pairs with an EDT main board (in a PCI, PCI-X, or PCIe bus), which adds high-speed DMA, programmable FPGA resources, and memory
- Channels 0 and 1 (input) and Channel 2 (output): One ECL data bit per channel
- Clocks: Channels 0 and 1 can each receive, and channel 2 can locally generate, a clock of up to 400 MHz
- FPGAs: One programmable Xilinx Virtex II Pro XC2VP2
- Reed-Solomon coding or raw serial data
- Two user-defined LEDs

Applications

- Telemetry receiver and transmitter
- Communications monitoring (serial data)
- Satellite ground station support

Specifications

Product Type	SSE is a mezzanine board for synchronous serial ECL; it requires a main board.			
FPGAs and Memory	One programmable FPGA (Xilinx Virtex II Pro XC2VP2), plus FPGA and memory resources on main board			
Clocks	Channel 0 - input	Can receive a clock of up to 400 MHz		
	Channel 1 - input	Can receive a clock of up to 400 MHz		
	Channel 2 - output	Can locally generate a clock of up to 400 MHz		
Data Rates	Data rates are dependent on data format and main board.			
Data Format (I/O)	Three channels are included (two input and one output), supporting the data formats and specifications shown below.			
		For data	**For clock**	**Termination**
	Channel 0 - input	One ECL differential pair	One ECL differential pair	50 Ω to -2 V
	Channel 1 - input	One ECL differential pair	One ECL differential pair	50 Ω to -2 V
	Channel 2 - output	One ECL differential pair	One ECL differential pair	—
Reed-Solomon Coding	Standard	CCSDS (255,223) with 5-way interleave depth		
	Frame synchronizer	32-bit pattern and 32-bit mask		
	Frames — check and flywheel	Up to 15 of each		
Connectors	One 15-pin D			
Cabling	Consult EDT for purchase options.			
Physical	Weight	3.1 oz. typical		
	Dimensions	6.6 x 4.2 x 0.5 in. (with a main board)		
Environmental	Temperature	Operating 0° to 40° C		
		Non-operating -40° to 70° C		
	Humidity	Operating 1% to 90%, non-condensing at 40° C		
		Non-operating 95%, non-condensing at 45° C		
System and Software	For details on system requirements and EDT-provided software driver packages, see specifications for your EDT main board.			

Support

EDT offers engineer-to-engineer customer support, from phone consultation to custom design of hardware, firmware, and software. Contact us for options and details.

Contact

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Ordering Options

- Main board: PCI SS / PCI GS / PCIe8 LX

For more options, see main board datasheet.