edt
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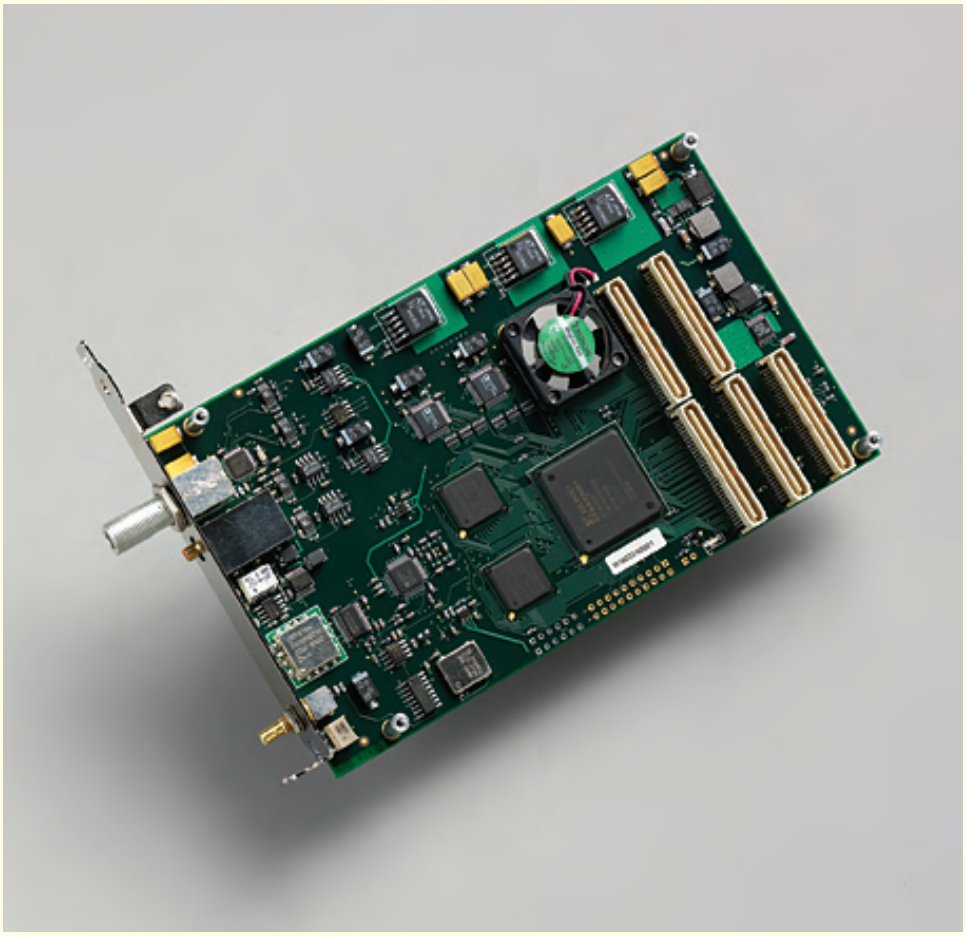
# SRXL

## Signal receiver and processor for L-band and IF



## Description

The SRXL is a mezzanine board that pairs with an EDT main board (for PCI or PCI Express) to accept simultaneous RF inputs in the L-band range of 925 to 2175 MHz and the IF range of 65 to 225 MHz.

Each input is processed with a tunable quadrature down-converter. The resulting baseband I and Q signals are low-pass filtered and digitized with 12-bit precision at programmable sample rates up to 65 MHz.

The resulting four channels of digital sample data are available as inputs to the Xilinx Spartan 3 FPGA, which is programmable to perform signal processing or to serve as a configurable switch matrix to route data to the main board and up to two 4-channel digital down-converter Graychips (GC4016).

The main board supplies high-speed DMA, plus additional memory and programmable FPGA resources.

## Features

- Mezzanine board – pairs with an EDT main board (in a PCI, PCI-X, or PCIe bus), which adds high-speed DMA, programmable FPGA resources, and memory
- Simultaneous L-band and IF analog-to-digital conversion (12-bit)
- L-band: 925 to 2175 MHz (66 MHz bandwidth) with 5 MHz tuning resolution
- IF: 65 to 225 MHz (46 MHz bandwidth) with 1 MHz tuning resolution
- FPGA: One programmable Xilinx Spartan 3 XC3S1500
- Graychips: Two optional (TI GC4016) for 8-channel digital down-conversion
- Sample clock: Programmable to any frequency from 1 to 65 MHz
- Reference clock: Onboard 10 MHz TCXO or optional external reference input

## Applications

- Satellite receiver
- Software-defined radio
- Surveillance / spectrum monitoring
- Digital tuning
- Test and measurement equipment

# Specifications

| | | | | |
|---|---|---|---|---|
| **Product Type** | SRXL is a signal receiver mezzanine board for L-band and IF; it requires a main board. | | | |
| **FPGAs and Memory** | One programmable FPGA (Xilinx Spartan 3 XC3S1500), plus FPGA and memory resources on main board | | | |
| **Graychips** | Two programmable or optional none (TI GC4016) for digital down-conversion | | | |
| **Sample Clock and Converter (A/D)** | Sample clock tuning range / tuning word (DDS) | 1 to 65 MHz / 32-bit word | | |
| | User-defined sample clock | From FPGA pin phase-locked to 10 MHz reference | | |
| | Converter resolution | 12 bits | | |
| **Data Rates** | Data rates are dependent on data format and main board. | | | |
| **Data Format (I/O)** | **General** | **Reference - External (10 MHz)** | **L-band (925-2175 MHz, 5 MHz tuning resolution)** | **IF (65-225 MHz, 1 MHz tuning resolution)** |
| | Nominal input impedance | 50 Ω | 75 Ω | 75 Ω |
| | Minimum return loss | 12 dB | 12 dB | 12 dB |
| | **Gain control** | | | |
| | Minimum RF | - | 60 dB | - |
| | Minimum base band | - | 19 dB | - |
| | Minimum variable | - | - | 43 dB |
| | Typical variable | - | - | 60 dB |
| | **Signal level** | | | |
| | Minimum usable | -10 dB | –72 dBm | –76 dBm |
| | Maximum usable | 10 dB | 3 dBm | –19 dBm |
| | Absolute maximum | 16 dBm (with DC, if any) | 10 dBm | 10 dBm |
| | **Phase noise** | | | |
| | At 40 KHz (measured) | - | -72 dB | -72 dB |
| | At 10 KHz (measured) | - | -50 dB | -65 dB |
| | **Local Oscillators** | | | |
| | Tuning ranges | - | 925 to 2175 MHz | 63 to 112 MHz or 125 to 225 MHz |
| | Tuning step size | - | 5 MHz | 1 MHz |
| | **Demodulators** | | | |
| | Base band LP filter cutoff | - | 4 to 33 MHz (–3 dB) | 23 MHz |
| | Transition band | - | 42 dB/octave | 24 dB/octave |
| | Maximum IQ phase error | - | 4 degrees | 3 degrees |
| | Maximum IQ gain error | - | 1.2 dB | 0.6 dB |
| **Reference - Internal** | **Frequency** | **Reference - Internal (10 MHz)** | | |
| | Nominal tolerance | +/- 0.5 ppm at 25° C | | |
| | Over temperature | +/- 2.5 ppm at 0° to 75° C | | |
| | Adjustment range | +/- 3 ppm | | |
| **Connectors** | | **Reference - External** | **L-band** | **IF** |
| | Connector type | SMB 50 Ω | F-type 75 Ω | SMB 75 Ω |
| **Cabling** | Consult EDT for purchase options. | | | |
| **Physical** | Weight | 3.6 oz. typical | | |
| | Dimensions | 6.6 x 4.2 x 0.5 in. (with a main board) | | |
| **Environmental** | Temperature | Operating 0° to 40° C | | |
| | | Non-operating -40° to 70° C | | |
| | Humidity | Operating 1% to 90%, non-condensing at 40° C | | |
| | | Non-operating 95%, non-condensing at 45° C | | |
| **System and Software** | For details on system requirements and EDT-provided software driver packages, see specifications for your EDT main board. | | | |

## Support

EDT offers engineer-to-engineer customer support, from phone consultation to custom design of hardware, firmware, and software. Contact us for options and details.

## Contact

**Engineering Design Team (EDT), Inc.**
1400 NW Compton Drive, Suite 315
Beaverton, Oregon 97006
800-435-4320 / 503-690-1234 (phone)
503-690-1243 (fax)
www.edt.com

## Ordering Options

- Main board: PCI SS / PCI GS / PCIe8 LX
- Graychips: 0 / **2**

**Bold** is default. For more options, see main board datasheet. **Ask about custom options.**