Description

The SRXL is a mezzanine board that pairs with an EDT main board (for PCI or PCI Express) to accept simultaneous RF inputs in the L-band range of 925 to 2175 MHz and the IF range of 65 to 225 MHz.

Each input is processed with a tunable quadrature down-converter. The resulting baseband I and Q signals are low-pass filtered and digitized with 12-bit precision at programmable sample rates up to 65 MHz.

The resulting four channels of digital sample data are available as inputs to the Xilinx Spartan 3 FPGA, which is programmable to perform signal processing or to serve as a configurable switch matrix to route data to the main board and up to two 4-channel digital down-converter Graychips (GC4016).

The main board supplies high-speed DMA, plus additional memory and programmable FPGA resources.

Features

- Mezzanine board – pairs with an EDT main board (in a PCI, PCI-X, or PCIe bus), which adds high-speed DMA, programmable FPGA resources, and memory
- Simultaneous L-band and IF analog-to-digital conversion (12-bit)
- L-band: 925 to 2175 MHz (66 MHz bandwidth) with 5 MHz tuning resolution
- IF: 65 to 225 MHz (46 MHz bandwidth) with 1 MHz tuning resolution
- FPGA: One programmable Xilinx Spartan 3 XC3S1500
- Graychips: Two optional (TI GC4016) for 8-channel digital down-conversion
- Sample clock: Programmable to any frequency from 1 to 65 MHz
- Reference clock: Onboard 10 MHz TCXO or optional external reference input

Applications

- Satellite receiver
- Software-defined radio
- Surveillance / spectrum monitoring
- Digital tuning
- Test and measurement equipment
### Specifications

**Product Type**  
SRXL is a signal receiver mezzanine board for L-band and IF; it requires a main board.

**FPGAs and Memory**  
One programmable FPGA (Xilinx Spartan 3 XC3S1500), plus FPGA and memory resources on main board

**Graychips**  
Two programmable or optional none (T1 GC4016) for digital down-conversion

**Sample Clock and Converter (A/D)**  
Sample clock tuning range / tuning word (DDS)  
User-defined sample clock  
Converter resolution  
1 to 65 MHz / 32-bit word  
From FPGA pin phase-locked to 10 MHz reference  
12 bits

**Data Rates**  
Data rates are dependent on data format and main board.

<table>
<thead>
<tr>
<th>Data Format (I/O)</th>
<th>General</th>
<th>Reference - External</th>
<th>L-band (925-2175 MHz, 5 MHz tuning resolution)</th>
<th>IF (65-225 MHz, 1 MHz tuning resolution)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Nominal input impedance</td>
<td>50 Ω</td>
<td>75 Ω</td>
<td>75 Ω</td>
</tr>
<tr>
<td></td>
<td>Minimum return loss</td>
<td>12 dB</td>
<td>12 dB</td>
<td>12 dB</td>
</tr>
<tr>
<td><strong>Gain control</strong></td>
<td>Minimum RF</td>
<td>-</td>
<td>60 dB</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td>Minimum base band</td>
<td>-</td>
<td>19 dB</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td>Minimum variable</td>
<td>-</td>
<td>-</td>
<td>43 dB</td>
</tr>
<tr>
<td></td>
<td>Typical variable</td>
<td>-</td>
<td>-</td>
<td>60 dB</td>
</tr>
<tr>
<td><strong>Signal level</strong></td>
<td>Minimum usable</td>
<td>-10 dB</td>
<td>-72 dBm</td>
<td>-76 dBm</td>
</tr>
<tr>
<td></td>
<td>Maximum usable</td>
<td>10 dB</td>
<td>3 dBm</td>
<td>-19 dBm</td>
</tr>
<tr>
<td></td>
<td>Absolute maximum</td>
<td>16 dBm (with DC, if any)</td>
<td>10 dBm</td>
<td>10 dBm</td>
</tr>
<tr>
<td><strong>Phase noise</strong></td>
<td>At 40 KHz (measured)</td>
<td>-</td>
<td>-72 dB</td>
<td>-72 dB</td>
</tr>
<tr>
<td></td>
<td>At 10 KHz (measured)</td>
<td>-</td>
<td>-50 dB</td>
<td>-65 dB</td>
</tr>
<tr>
<td><strong>Local Oscillators</strong></td>
<td>Tuning ranges</td>
<td>-</td>
<td>925 to 2175 MHz</td>
<td>63 to 112 MHz or 125 to 225 MHz</td>
</tr>
<tr>
<td></td>
<td>Tuning step size</td>
<td>-</td>
<td>5 MHz</td>
<td>1 MHz</td>
</tr>
<tr>
<td><strong>Demodulators</strong></td>
<td>Base band LP filter cutoff</td>
<td>-</td>
<td>4 to 33 MHz (-3 dB)</td>
<td>23 MHz</td>
</tr>
<tr>
<td></td>
<td>Transition band</td>
<td>-</td>
<td>42 dB/octave</td>
<td>24 dB/octave</td>
</tr>
<tr>
<td></td>
<td>Maximum IQ phase error</td>
<td>-</td>
<td>4 degrees</td>
<td>3 degrees</td>
</tr>
<tr>
<td></td>
<td>Maximum IQ gain error</td>
<td>-</td>
<td>1.2 dB</td>
<td>0.6 dB</td>
</tr>
</tbody>
</table>

**Reference - Internal**  
**Frequency**  
Nominal tolerance +/- 0.5 ppm at 25° C  
Over temperature +/- 2.5 ppm at 0° to 75° C  
Adjustment range +/- 3 ppm

<table>
<thead>
<tr>
<th>Connectors</th>
<th>Connector type</th>
<th>Reference - External</th>
<th>L-band 75 Ω</th>
<th>IF 75 Ω</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>SMB 50 Ω</td>
<td>F-type 50 Ω</td>
<td>12 dB</td>
<td>12 dB</td>
</tr>
</tbody>
</table>

**Cabling**  
Consult EDT for purchase options.

**Physical**  
Weight 3.6 oz. typical  
Dimensions 6.6 x 4.2 x 0.5 in. (with a main board)

**Environmental**  
Temperature Operating 0° to 40° C  
Non-operating -40° to 70° C  
Operating 1% to 90%, non-condensing at 40° C  
Non-operating 95%, non-condensing at 45° C

**Humidity**  
Operating 1% to 90%, non-condensing at 40° C  
Non-operating 95%, non-condensing at 45° C

**System and Software**  
For details on system requirements and EDT-provided software driver packages, see specifications for your EDT main board.

### Support

EDT offers engineer-to-engineer customer support, from phone consultation to custom design of hardware, firmware, and software. Contact us for options and details.

### Contact

**Engineering Design Team (EDT), Inc.**  
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Beaverton, Oregon 97006  
800-435-4320 / 503-690-1234 (phone)  
503-690-1243 (fax)  
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### Ordering Options

- Main board: PCI SS / PCI GS / PCIe8 LX  
- Graychips: 0 / 2

**Bold** is default. For more options, see main board datasheet. Ask about custom options.