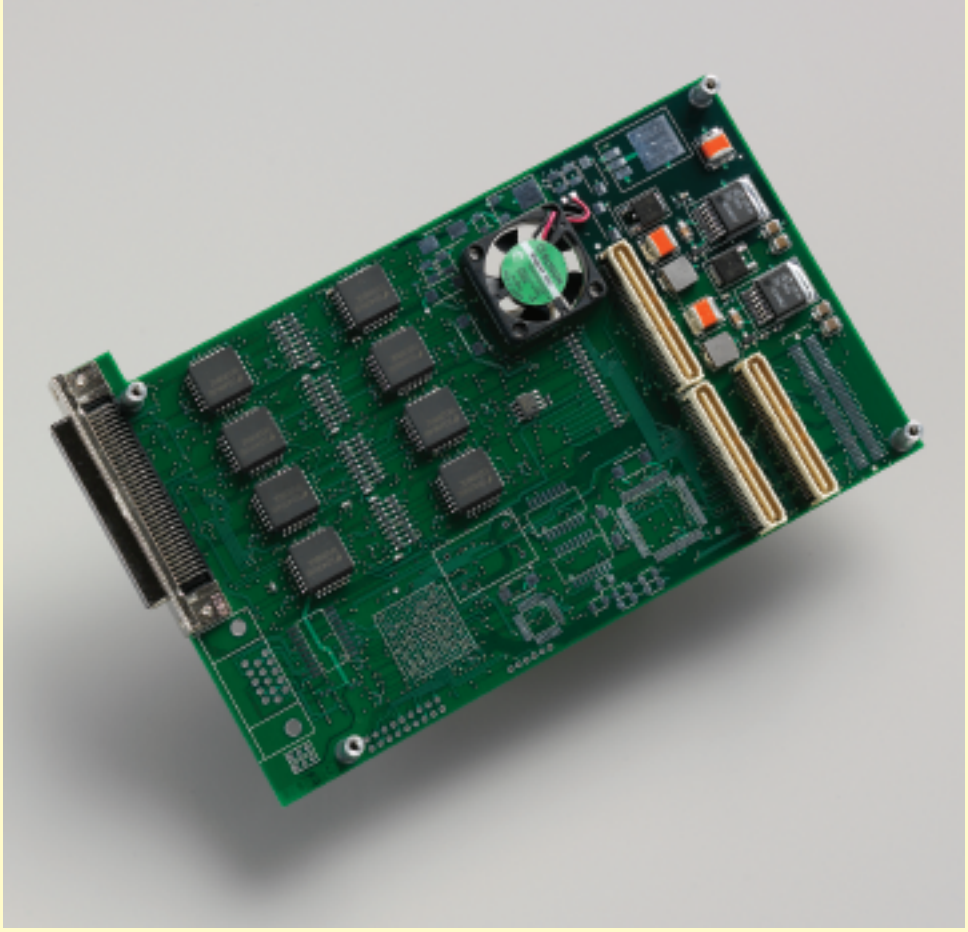
edt
a HEICO company

PCI SS/GS ECL



Features

- 32 ECL input/output signals
- Transfer rates up to 60 megabits per second per signal
- User-programmable FPGA up to Xilinx XCV2000E (PCI SS) or XC2VP70 (PCI GS)
- Local memory up to 1 gigabyte (PCI GS)
- LVDS external clock that can be used to synchronize the output data
- Single short PCI local bus slot
- Fast transfers using a 66 MHz 32-bit PCI
- Configuration files for 16 synchronous serial channels
- Optional two T1/E1 input/output channels
- Optional SSE two simultaneous input channels and one output channel (400 megabit per second synchronous serial ECL)

Description

The ECL mezzanine board provides 32 differential ECL interface signals for either the PCI SS or PCI GS main boards. The ECL signals can be inputs or outputs in groups of four (two channels). The function of each signal is determined by the FPGA configuration file used on the main board.

The ECL mezzanine board is supplied with FPGA configuration files that implement 16 synchronous serial channels. Each channel inputs or outputs a data signal on the edge of the associated clock. The data is stored in or sent from host memory using the PCI DMA. This configuration provides a simple, flexible solution for telemetry, satellite, and monitoring applications.

A large Xilinx Virtex™-E (PCI SS) or Virtex™-II Pro (PCI GS) FPGA and associated memory allow the user to implement an FPGA configuration and process large amounts of serial ECL data. The separate high-speed 16-channel PCI DMA controller allows flexible access to host memory.

Applications

- Telemetry receiver and transmitter
- Monitoring serial data communications
- Satellite ground station support

Specifications

PCI Local Bus Compliance (when mounted on PCI SS/GS Main Board)	PCI Version	PCI 2.2
	Data Width	32 bits
	Number of Slots	1
	Transfer Size	Up to 1024 bytes per transfer
	DMA (Direct Memory Access)	Yes
	PCI Local Bus Memory Space	Approximately 66 KB
	Clock Rate	33 MHz or 66 MHz
External Connectors	High-density 68-pin AMP™ connector (part number 787169-7)	
ECL	32 differential ECL signals; input or output in groups of four Standard ECL signal levels, terminated through 50 ohms to -2V	
Physical	Number of Slots	1
	Dimensions	4.2" x 6.6"
Environmental	Temperature	Operating: 0° to 40° C Non-operating: –40° to 70° C
	Humidity	Operating: 1% to 90% non-condensing at 40° C Non-operating: 95% non-condensing at 45° C
System Requirements	Intel, AMD, SPARC, or PowerPC computer with 66 MHz PCI Bus or faster (will run in 33 MHz slot with reduced performance)	

Software

Device Drivers for Solaris 2.7+ (Intel and SPARC platform), Windows NT/XP/2000/-2003, Red Hat Linux 9.0, Red Hat Enterprise v3-v4, SuSE Linux 9.1-10, are included with the board. Mac OS X and VxWorks drivers are also available.

Support

EDT provides engineer-to-engineer customer support, from phone consultation to custom design of hardware, firmware, or software. Technical support is also available through the Technical Information section of our web site.

Ordering

Ordering options are listed below. To order, contact our sales department or your distributor. Be sure to specify which cable will be needed (if any).

PCI SS ECL

Option: **32 differential ECL signals** or two T1/E1 output channels

Interface option: SSE (see PCI SS/GS data sheet for more information)

PCI GS ECL

Option: two T1/E1 output channels

Interface option: SSE (see PCI SS/GS data sheet for more information)

See PCI SS and PCI GS data sheets for main board options.

Bold denotes standard

Contact

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