edt
a HEICO company

PCI GS

PCI high-speed DMA and data processing interface - v. 2

Description

The PCI GS (for PCI) is a main board that provides powerful high-speed DMA, memory, and programmable FPGA resources. It is designed to support any one of numerous EDT mezzanine boards.

The PCI GS has a programmable FPGA (Xilinx Virtex II Pro XC2VP50 or XC2VP70, with two on-chip PowerPC processors) and synchronous memory of up to 8 MB SRAM and up to 1 GB 200-pin SODIMM DDR2 DRAM.

The board also has four independent programmable PLL clock generators, which can be set to select frequencies with less than +/- 50 ppm error.

An EDT Bridge is available to link two main boards together.

Features

- Main board (fits in a PCI or PCI-X bus) — supports an EDT mezzanine board with high-speed DMA, programmable FPGA resources, and memory
- 221 LVTTL programmable signals connected to mezzanine board
- FPGA: One programmable Xilinx Virtex II Pro XC2VP50/70 with two on-chip PowerPC processors
- SRAM: Up to 8 MB
- DRAM: Up to 1 GB (DDR2)
- Clocks: Four independent programmable PLL clock generators

Applications

EDT mezzanine board support on PCI or PCI-X platforms

Specifications

Product Type	PCI GS is a PCI main board (v. 2); it supplies DMA, memory, and programmable FPGA resources to a mezzanine board.	
FPGA Resources	One programmable FPGA (Xilinx Virtex II Pro XC2VP50 or optional 70) with two on-chip PowerPC processors	
Memory	SRAM DRAM (DDR2)	Dependent on FPGA selected (4 MB on XC2VP50; 8 MB on optional 70) 0 or optional 1 GB (200-pin SODIMM)
Clocks	Four programmable independent PLL clock generators, each with input and output clocks: Input (reference) clocks can be set to 10.3681 or 40 MHz, or PCI clock. Output clocks can be set with only +/- 50 ppm error to 1.544, 2.048, 6.312, 8.448, 34.368, or 44.736 MHz.	
Data Rates	Peak Typical	TBD TBD (dependent on mezzanine board, bus chipset, and host system)
Data Format (I/O)	Determined by mezzanine board and optional auxiliary board	
PCI Compliance	PCI version DMA Number of slots	PCI 2.3 1, 4, or 16 channels, depending on mezzanine board 1
Connectors	Five CMC-type (IEEE 1386) mezzanine One 6-pin .100" x 1 row square .025" One 8-pin .100" x 1 row square .025" square pins One 40-pin ATA-type expansion	221 LVTTL I/O (mate to AMP 120527-1 or Molex 71436-2164) For FPGA JTAG (IEEE 1149.1) For six external debugging LEDs 30 LVTTL signals for external board or FPGA debugging (8 can be used for Xilinx RocketIO)
Cabling	Consult EDT for purchase options.	
Physical	Weight Dimensions	4.2 oz. typical 6.6 x 4.2 x 0.5 in.
Environmental	Temperature Humidity	Operating 0° to 40° C Non-operating -40° to 70° C Operating 1% to 90%, non-condensing at 40° C Non-operating 95%, non-condensing at 45° C
System and Software	System must have a PCI or PCI-X bus, 66 MHz or faster (33 MHz will work, but at reduced data rates). Software is included for Windows, Solaris, Linux, and Mac OS X and can be requested for VxWorks; for versions, see our website.	

Support

EDT offers engineer-to-engineer customer support, from phone consultation to custom design of hardware, firmware, and software. Contact us for options and details.

Contact

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Ordering Options

- Mezzanine board: See Compatibility Guide.
- FPGA: XC2VP**50** / 70
- SRAM: **4 MB** / 8 MB (dependent on FPGA)
- DRAM: **0** / 1 GB

Bold is default. For more options, see mezzanine board datasheet. **Ask about custom options.**