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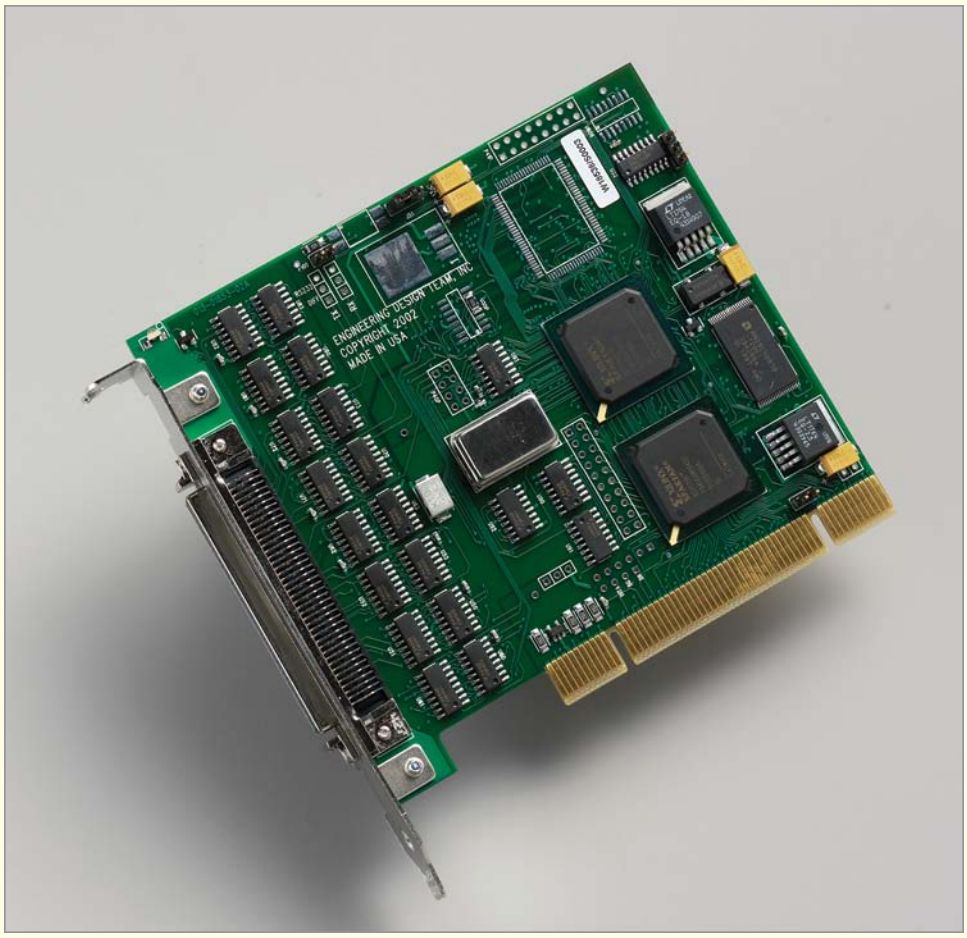
PCI CDa

PCI interface for high-speed DMA and synchronous I/O



Description

The PCI CDa is a PCI interface that provides fast DMA and asynchronous I/O to transfer data (RS422 or LVDS / EIA644) between an external device and a host computer.

The board provides a Xilinx Spartan IIE FPGA to enable one or multiple channels: either an XC2S100E for one 16-bit parallel channel, or an optional XC2S600E for two channels (8-bit parallel full duplex); eight channels (synchronous serial with data valid — encryption / decryption); or sixteen channels (synchronous serial).

Data rates (observed) are up to 210 MB/s for one channel, or up to 70 Mb/s per channel for sixteen channels.

The hardware protocol is synchronous: all data and control signals are sampled by a clock transmitted along with them. This sample clock can be generated by the DMA interface, the user device, or both.

All channels are VHDL in the user-interface FPGA. EDT allows access to the source VHDL for custom designs.

Features

PCI interface for high-speed DMA and asynchronous I/O between external device and host computer

Supports one, two, eight, or sixteen channels of DMA:
- One 16-bit parallel;
- Two 8-bit parallel (full duplex);
- Eight synchronous serial data valid with encryption / decryption; or
- Sixteen synchronous serial

FPGA: One user-programmable Xilinx Spartan IIE
- XC2S100E for single-channel operation; or
- Optional XC2S600E for multi-channel operation

I/O: RS422 or LVDS (EIA644)

Buffers: Integrated FIFOs for input and output

Clock: 33 or 66 MHz, 3- or 5-volt PCI-capable

Data rates: 210 MB/s (one channel) or 70 Mb/s per channel (sixteen channels)

Applications

Simulation

Imaging devices

Scanners

Plotters

Device control

General-purpose data acquisition

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Specifications

Product Type	PCI CDa is a PCI interface that provides high-speed DMA and asynchronous I/O for RS422 or LVDS.	
FPGA Resources	One programmable Xilinx Spartan IIE	XC2S100E (for one channel) or optional XC2S600E (for multiple channels)
Other Resources	Buffers	Integrated FIFOs for input and output
Memory	0	
Clock	1 PLL clock generator 66 or 33 MHz, 3- or 5-volt PCI-capable	
Data Rates	For one-channel operation For optional sixteen-channel operation	210 MB/s 70 Mb/s per channel
Data Format (I/O)	RS422 or LVDS	
Protocol	For one-channel, 16-bit parallel For sixteen-channel	Synchronous streaming Synchronous serial
PCI Compliance	PCI version DMA channels and transfer sizes Number of slots	PCI 2.3 One 16-bit parallel (up to 1024 bytes per transfer); optionally, two 8-bit parallel or eight or sixteen synchronous serial (up to 64 bytes per transfer) One
Configuration packages	XC2S100E FPGA XC2S600E FPGA	One-channel 16-bit parallel Two-channel 8-bit parallel (full duplex) Eight-channel synchronous serial (data valid – encryption / decryption) Sixteen-channel synchronous serial
Connectors	AMP 787190-8 high-density 80-pin (mates with AMP 749621-8, backshell 749196-2)	
Physical	Weight Dimensions	3.3 oz. typical 5.0 x 4.2 x 0.5 in.
Environmental	Temperature Humidity	Operating: 10° to 40° C Non-operating: -40° to 70° C Operating: 1% to 90%, non-condensing at 40° C Non-operating: 95%, non-condensing at 40° C
System and Software	System must have a PCI or PCI-X bus, 66 MHz or faster (33 MHz will work, but at reduced data rates). Software is included for Windows, Solaris, Linux, and Mac OS X; for versions, see our website.	

Ordering Options

- FPGA: **XC2S100E** / 600E (one / multichannel)
- I/O: **RS422** or LVDS
- DMA: **One-** or multi-channel

Bold is default. **Ask** about custom options.