









LEONARDO™ CL Digital Video Processor Line

The leonardo[™] line is the real solution for fast CameraLink[™] digital video acquisition and realtime processing of the incoming video data. The product line comes in several PCI, CompactPCI and PMC models based on a very strong architecture.

The common digital video interface is CameraLink[™] compatible, the formats ranging from Base, via Medium to Full CameraLink[™]. The computer bus interface is electrically compatible with PCI 2.2 and mechanically with standard PCI, Compact PCI and PMC. The bus interface is 64 bit/66 MHz, resulting in an extreme transfer rate of 528 MB/s on the computer bus.

The leonardo[™] is equiped with a state of the art Xilinx FPGA, offering realtime preprocessing of the video data, such as e.g. contrast stretching in gray value domain, RGB mosaic color restoration and random 2D convolution filters. The video data is stored in a very large on board memory. The maximum image resolution is 64k*64k pixels.

On the CL-P model an on board 600 MHz 64-bit RISC processor is available, with 4 MByte zero-waitstate SRAM cache memory. The RISC processor is specified as a 1080 Drystone 2.1 MIPS@600MHz. The RISC processor is available for general purpose application specific on board video processing.

The leonardo[™] CL family is supported for Windows^R, Linux, RT Linux, RT Linux Pro and QNX^R. The RISC processor is C programmable (CL-P model only).

Available models:	Camera	aLink™ in Medium		600 MHz RISC processor	cache	on board memory	bus
PCI64-CL	++	+	+			128 MB	PCI
PMC64-CL	+					128 MB	PMC
cPCI64-CL	#	+	+			128 MB	Compact PCI (3U)
PCI64-CL-P	#	+	+	+	4 MB	max 1 GB	PCI

++ = option for **DUAL** CameraLinkTM Base acquisition (Dual Base)



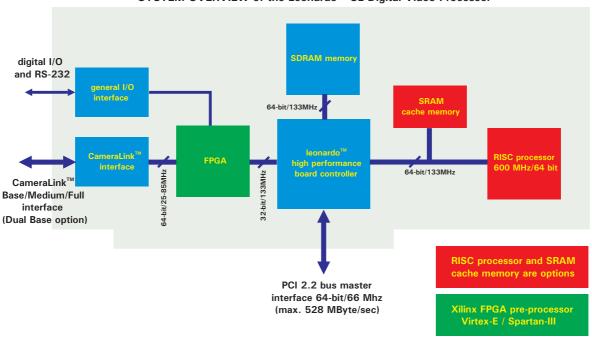
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LEONARDO™ CL

Features

SYSTEM OVERVIEW of the Leonardo™ CL Digital Video Processor



CameraLink [™] interface	Base 24 bit Medium 48 bit Full 64 bit	FPGA	Xilinx Virtex-E XCV 100E (option: Xilinx Spartan-III XC3S1000)	
	Dual Base 24 bit (optional)	DMA channels	8 channels with extended features	
Image size	64k*64k pixels max	SDRAM memory	128 MB default, optional 256 MB upto 1 GB DIMM on CL-P model	
Pixel clock (maximum)	8 bit-85 MHz 16 bit-85 MHz 32 bit-50 Mhz	Onboard Bus	133 MHz bus frequency max throughput 1.064 GByte/sec	
	40 bit-40 MHz 48 bit-25 MHz 64 bit-25 MHz	MIPS processor	64 bit 600 MHz RISC processor (PMC Sierra RM7000C default) 1080 Drystone 2.1 MIPS @ 600 Mhz 1600 MFLOPS floating point unit 16 kB instruction, 16 kB data and 256 kB secondary cache	
PCI controller	PCI 2.2 compatible Master / slave 3.3 and 5 Volt compatible			
PCI modes	64bit/66MHz 64bit/33MHz	Cache memory	4 MB external, only available when MIPS processor is mounted	
	32bit/33MHz	User I/O	2 isolated digital inputs 2 isolated digital outputs 2*RS-232 serial channels	
PCI Bustransfer	max. 528 MByte (approx. 480 MB sustained)			

for more technical details, please refer to the hardware manual



Ordering Information

Order code information leonardo™ CL series:

model: order code:

PCI64-CL XXX64-CL-mode-logic-temp-mem

PMC64-CL

cPCI64-CL PCI, PMC or cPCI (defines computer bus and board format) XXX

> FL - CameraLink Base-Medium-Full support (default) mode

DB - CameraLink Dual Base-Medium support

X100 - Xilinx Virtex-E XCV100E mounted (default) logic

X1000 - Xilinx Spartan-III XC3S1000 mounted

C - commercial temperature range, 0 to +70°C (default) temp

I - industrial temperature range, -40 to +85°C

mem 128 - 128 MByte SDRAM mounted (default)

256 - 256 MByte SDRAM mounted

example: PCI64-CL-FL-X100-C-256

defines a PCI model with all default options, but 256 MB SDRAM

PCI64-CL-P PCI64-CL-P-mode-logic-temp-mem

> FL - CameraLink Base-Medium-Full support (default) mode

> > DB - CameraLink Dual Base-Medium support

X100 - Xilinx Virtex-E XCV100E mounted (default) logic C - commercial temperature range, 0 to $+70^{\circ}$ C (default) temp

I - industrial temperature range, -40 to +85°C

256 - 256 MByte SDRAM mounted (default) mem

*** - other value, max 1 GB SDRAM

example: PCI64-CL-P-DB-X100-I-512

defines a CL-P board with RISC processor, cache memory and 512 MB SDRAM mounted, supporting CameraLink Dual Base-Medium and

industrial temperature

Important remark, industrial temperature limitations: on board bus running at 100 MHz, limited SDRAMsize, RM7000A at 350 MHz mounted, max camera pixelclock 66 Mhz, for availablity of industrial temperature range models please contact ARVOO or your local distributor

This brochure revision replaces all previous revisions and product specifications.

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Your local distributor:



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