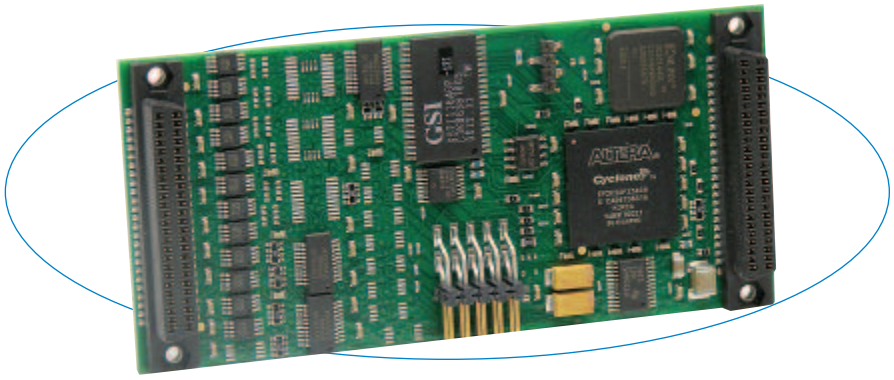
Acromag
THE LEADER IN INDUSTRIAL I/O

IP-EP200 JTAG-Reconfigurable Cyclone™ II FPGA Digital I/O Modules



These modules support adaptive computing applications with an FPGA running custom programs to control system communication.

This series of plug-in mezzanine modules provides a user-customizable Altera® Cyclone II FPGA on an Industry Pack (IP) module. The module allows users to develop and store their own instruction set in the FPGA for adaptive computing applications. Typical uses include specialized communication systems over RS422/485 networks, test fixture simulation of signals over TTL-switched lines, and analysis of acquired data using specialized mathematical formulas such as those developed with MathWorks's MatLab® software.

The FPGA on Acromag's IP-EP200 modules can control up to 48 TTL or 24 RS485 I/O signals or a mix of both types. Another model interfaces 24 LVDS I/O channels. User application programs are downloaded through the JTAG port or via the IP bus directly into the FPGA. A pre-programmed internal CPLD facilitates initialization by acting as the bus controller during power-up and while the program is downloading. This bus controller is limited to functions necessary for power-up and down-loading. After the program downloads, the FPGA takes control of the IP bus and the CPLD disables.

Features

- Altera Cyclone II EP2C20 FPGA
- Four models available:
  IP-EP201: 48 TTL I/O lines
  IP-EP202: 24 differential RS485 I/O lines
  IP-EP203: 24 TTL and 12 RS485 I/O lines
  IP-EP204: 24 LVDS I/O lines
- FPGA programmable via JTAG port or IP bus
- Local static RAM (64K x 16) under FPGA control
- LVTTL external clock connected directly to the FPGA
- Supports 8MHz and 32MHz IP bus
- Programmable PLL-based clock synthesizer
- Example FPGA design code provided as VHDL
  - 8MHz IP bus interface
  - Digital I/O control register
  - others
- Hardware support for DMA and memory space

Specifications

FPGA

FPGA: Altera Cyclone II EP2C20.

FPGA configuration: Downloadable via JTAG port or IP bus.

Clock: Cypress CY22150 (or equivalent).
Generates frequencies from 250kHz to 100MHz

Input/output signals:
IP-EP201: 48 TTL lines
IP-EP202: 24 differential RS485 lines
IP-EP203: 24 TTL lines and 12 RS485
IP-EP204: 24 LVDS lines
All models: LVTTL external clock input

IP bus clock frequency: Supports 8 and 32MHz clocks.

ID space: 8-bit data.

I/O space: 8 or 16-bit data.

Memory space: Wired to FPGA but not supported with example FPGA design firmware.

Interrupt support: Two IP request levels.

DMA support: Wired to FPGA but not supported with example FPGA design firmware.

IP logic interface: CPLD maintains ID space and two locations in IO space for FPGA configuration. Remaining IO space and INT space are defined by the configured FPGA.

Example FPGA program: VHDL provided implements IP bus interface to IO, ID, and INT space. Requires user proficiency with VHDL and Altera Quartus® II software tools. See Engineering Design Kit.

IP Compliance (ANSI/VITA 4)

Meets IP specifications per ANSI/VITA 4-1995.

IP data transfer cycle types supported: Input/output (IOSel*), ID read (IDSel*), Interrupt select (INTSel*).

Access times (8MHz or 32MHz clock):
ID space read: 1 wait state (375nS cycle @ 8MHz).
Registers read/write: 1 wait state (375nS cycle @ 8MHz).
Interrupt read/write: 1 wait state (375nS cycle @ 8MHz).

Environmental

Operating temperature: 0 to 70°C or -40 to 85°C (E models).

Storage temperature: -55 to 125°C.

Relative humidity: 5 to 95% non-condensing.

MTBF: Consult factory.

Engineering Design Kit

Engineering Design Kit: Provides user with basic information required to develop a custom FPGA program for download to the Altera FPGA. This kit must be ordered with the first purchase of an IP-EP200 module.
Kit on CD-ROM includes:
Schematics (.pdf)
Parts list and part location drawing (.pdf)
Example VHDL source file (.vhd)
Example assignments file (.qsf)
Example configuration file (.hex)
Programming guide (.pdf)

Only one Design Kit purchase is required. User should be fluent in use of Altera Quartus design tools. Additionally, user should also purchase either the IPSW-API-VXW (VxWorks source code library) or the IPSW-API-WIN (Windows DLL driver package). These programs include important driver support programs to assist in transferring developer code between user's processor and EPC20 FPGA.

Ordering Information

Industry Pack Modules

IP-EP201: 48 TTL I/O lines

IP-EP201E: Same as above w/extended temperature range

IP-EP202: 24 differential RS485 I/O lines

IP-EP202E: Same as above w/extended temperature range

IP-EP203: 24 TTL and 12 RS485 I/O lines

IP-EP203E: Same as above w/extended temperature range

IP-EP204: 24 LVDS I/O lines

IP-EP204E: Same as above w/extended temperature range

IP-EP2-EDK: Engineering Design Kit (one kit required)

Acromag offers a wide selection of Industry Pack Carrier Cards.

Software *(see software documentation for details)*

IPSW-API-VXW: VxWorks® software support package

IPSW-API-QNX: QNX® software support package

IPSW-API-WIN: Windows® DLL driver software support pkg.

IPSW-LINUX: Linux™ support (website download only)

See accessories documentation for additional information.

Acromag, Inc. • PO Box 437, Wixom, MI 48393 • Phone: 248-295-0310 • Fax: 248-624-9234 • solutions@acromag.com • www.acromag.com