XMC Modules

XMC-7A200CC User-Configurable Conduction-Cooled Artix®-7 FPGA Modules

Description

Acromag's XMC-7A200CC modules feature a high-performance user-configurable Xilinx® Artix®-7 FPGA enhanced with high-speed memory and a high-throughput serial bus interface. The result is a powerful and flexible I/O processor module that is capable of executing custom instruction sets and algorithms.

The logic-optimized FPGA is well-suited for a broad range of applications. Typical uses include hardware simulation, communications, in-circuit diagnostics, military servers, signal intelligence, and image processing.

The rear I/O provides an 8-lane high-speed serial interface on the P16 XMC port for customer-installed soft cores. P16 also supports 34 SelectIO channels. The P4 port adds another 60 SelectIO and global clock lines. SelectIO signals are Artix-7 FPGA I/O pins that support single-ended I/O (LVCMOS, HSTL, SSTL) and differential I/O standards (LVDS, HT, LVPECL, BLVDS, HSTL, SSTL).

With Acromag's Artix-7 FPGA modules, you can greatly increase DSP algorithm performance for faster throughput using multiple channels and parallel hardware architectures. Free up CPU cycles by offloading algorithmic-intensive tasks to the FPGA co-processor.

These modules are ideal for high-performance customized embedded systems. Optimize your system performance by integrating high-speed programmable logic with the flexibility of software running on MicroBlaze™ soft processors.

Acromag's Engineering Design Kit provides software utilities and example VHDL code to simplify your program development and get you running quickly. A JTAG interface enables on-board debugging. Additional Xilinx tools help finish your system faster. Maximize FPGA performance with Vivado® or ISE® Design Suite. And with ChipScope™ Pro tools, you can rapidly debug logic and serial interfaces.

Key Features & Benefits

- Reconfigurable Xilinx Artix-7 FPGA with 215K logic cells
- 128M x 64-bit DDR3 SDRAM
- 32M x 16-bit parallel flash memory for MicroBlaze FPGA program code storage
- 4-lane high-speed serial interface on rear P15 connector for PCIe Gen 1/2 (standard), Serial RapidI/O, 10Gb Ethernet, Xilinx Aurora
- 8-lane high-speed interfaces on rear P16 connector for customer-installed soft cores
- 60 SelectIO or 30 LVDS pairs plus 2 global clock pairs direct to FPGA via rear P4 port
- 34 SelectIO or 17 LVDS pairs plus 2 global clock pairs direct to FPGA via rear P16 port
- DMA support provides data transfer between system memory and the on-board memory
- Support for Xilinx ChipScope™ Pro interface
- Extended temperature conduction-cooled

XMC module with PCIe interface ◆ Logic-optimized Artix 7 FPGA ◆ Conduction-Cooled
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Performance Specifications

- **FPGA**
  - FPGA device
  - Xilinx Artix-7 FPGA.
  - Model XC7A200T FPGA with 215,360 logic cells and 740 DSP48E1 slices.
  - FPGA configuration
    - Download via JTAG or flash memory.
  - Example FPGA program
    - IP integrator block diagram provided for bus interface, front & rear I/O control, and SDRAM memory interface controller. See EDK kit.

- **I/O Processing**
  - Rear high-speed I/O
    - 12 high-speed serial lanes.
    - x4 lanes via P15 and x8 lanes via P16.
  - Rear user I/O
    - P16: 17 LVDS pairs (34 LVCMOS), 2 global clock pairs.
    - P4: 30 LVDS pairs (60 LVCMOS), 2 global clock pairs.

- **Engineering Design Kit**
  - Provides user with basic information required to develop a custom FPGA program. Kit must be ordered with the first purchase of a XMC-7 series module (see www.acromag.com for more information).

- **XMC Compliance**
  - Complies with ANSI/VITA 42.0 specification for XMC module mechanicals and connectors.
  - Complies with ANSI/VITA 42.3 specification for XMC modules with PCI Express interface.
  - Electrical/Mechanical Interface: Single-Width Module.

- **Electrical**
  - XMC PCIe bus interface (P15 and P16)
    - One 114-pin male connector (Samtec ASP-103614-05 or equivalent).
  - P15 primary XMC connector
    - 4 differential pairs (PCIe standard, Serial RapidIO, 10-Gigabit Ethernet, or Xilinx Aurora). JTAG.
    - System Management (XMC provides hardware definition information read by an external controller using IPMI commands and I2C serial bus transactions.)
    - 3.3V power: 4 pins at 1A/pin.
    - 3.3V auxiliary power: 1 pin, powers volatile memory to store the bitstream encryption key. Variable power (5V or 12V): 8 pins at 1A per pin.
  - P16 XMC connector
    - 8 differential pairs (PCIe, Serial RapidIO, or Xilinx Aurora).
    - 17 LVDS pairs or 34 SelectI/O signals (differential pairs grouped per VITA 46.0 X38s).
    - 2 global clock pairs.
    - Vcco pins are powered by 2.5V and support the 2.5V I/O standards.
  - P4 PMC rear I/O connector
    - 64-pin female receptacle header (AMP 120527-1 or equivalent).
    - 64 I/O connections (30 LVDS pairs plus two global clocks).
    - Vcco pins powered by 2.5V and support the 2.5V I/O standards.

- **Environmental**
  - Operating temperature
    - XMC-7A200CC-LF: Conduction-cooled, -40 to 75°C.
  - Storage temperature
    - -55 to 125°C.
  - Relative humidity
    - 5 to 95% non-condensing.
  - Power
    - 3.3V (±5%): 7W typical.
    - 12V (±5%): 2W typical.
    - 3.3V AUX (±5%): 57µW
  - MTBF
    - Contact the factory.

Ordering Information

- NOTE: XMC-7KA-EDK is required to configure FPGA.

- **XMC Modules**
  - XMC-7A200CC-LF
    - User-configurable Artix-7 FPGA, 215k logic cells, conduction-cooled

- **Software**
  - For more information, see www.acromag.com.
  - XMC-7KA-EDK
    - Engineering Design Kit (one kit required)
  - PMCSW-API-VXW
    - VxWorks® 32-bit software support package
  - PCISW-API-WIN
    - Windows® DLL software support package
  - PCISW-API-LNX
    - Linux® support (website download only)

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