Description
Acromag’s XMC-7A modules feature a high-performance user-configurable Xilinx® Artix®-7 FPGA enhanced with high-speed memory and a high-throughput serial bus interface. The result is a powerful and flexible I/O processor module that is capable of executing custom instruction sets and algorithms.

The logic-optimized FPGA is well-suited for a broad range of applications. Typical uses include hardware simulation, communications, in-circuit diagnostics, military servers, signal intelligence, and image processing.

Both front and rear I/O is supported. Front I/O processing is supported with plug-in AXM mezzanine cards. A variety of AXM I/O cards are available to add the flexibility of a wide range of analog and digital I/O to your design.

The rear I/O provides an 8-lane high-speed serial interface on the P16 XMC port for customer-installed soft cores. P16 also supports 34 SelectIO channels. The P4 port adds another 60 SelectIO and global clock lines. SelectIO signals are Artix-7 FPGA I/O pins that support single-ended I/O (LVCMOS, HSTL, SSTL) and differential I/O standards (LVDS, HT, LVPECL, BLVDS, HSTL, SSTL).

With Acromag’s Artix-7 FPGA modules, you can greatly increase DSP algorithm performance for faster throughput using multiple channels and parallel hardware architectures. Free up CPU cycles by offloading algorithmic-intensive tasks to the FPGA co-processor.

These modules are ideal for high-performance customized embedded systems. Optimize your system performance by integrating high-speed programmable logic with the flexibility of software running on MicroBlaze™ soft processors.

Acromag's Engineering Design Kit provides software utilities and example VHDL code to simplify your program development and get you running quickly. A JTAG interface enables on-board debugging. Additional Xilinx tools help finish your system faster. Maximize FPGA performance with Vivado® or ISE® Design Suite. And with ChipScope™ Pro tools, you can rapidly debug logic and serial interfaces.

Key Features & Benefits
- Reconfigurable Xilinx Artix-7 FPGA with 200k logic cells
- 128M x 64-bit DDR3 SDRAM
- 32M x 16-bit parallel flash memory for MicroBlaze FPGA program code storage
- 4-lane high-speed serial interface on rear P15 connector for PCIe Gen 1/2 (standard), Serial RapidIO, 10Gb Ethernet, Xilinx Aurora
- 8-lane high-speed interfaces on rear P16 connector for customer-installed soft cores
- 60 SelectIO or 30 LVDS pairs plus 2 global clock pairs direct to FPGA via rear P4 port
- 34 SelectIO or 17 LVDS pairs plus 2 global clock pairs direct to FPGA via rear P16 port
- DMA support provides data transfer between system memory and the on-board memory
- Support for Xilinx ChipScope™ Pro interface
### Performance Specifications

- **FPGA**
  - FPGA device
  - Xilinx Artix®-7 FPGA
  - Model XCA7A200T FPGA with 215,360 logic cells and 740 DSP48E1 slices.
  - FPGA configuration: Download via JTAG or flash memory.
  - Example FPGA program: IP integrator block diagram provided for bus interface, front & rear I/O control, and SDRAM memory interface controller. See EDK kit.

- **I/O Processing**
  - Acromag AXM I/O Modules: AXM modules plug into the XMC module's front mezzanine for additional I/O lines. Analog and digital I/O AXM modules are sold separately.
  - Rear high-speed I/O:
    - 12 high-speed serial lanes.
    - x8 lanes via P15 and x8 lanes via P16.
  - Rear user I/O:
    - P16: 17 LVDS pairs (34 LVCMOS), 2 global clock pairs.
    - P4: 30 LVDS pairs (60 LVCMOS), 2 global clock pairs.

- **Engineering Design Kit**
  - Provides user with basic information required to develop a custom FPGA program. Kit must be ordered with the first purchase of a XMC-7A module (see www.acromag.com for more information).

- **XMC Compliance**
  - Complies with ANSI/VITA 42.0 specification for XMC module mechanicals and connectors.
  - Complies with ANSI/VITA 42.3 specification for XMC modules with PCI Express interface.
  - Electrical/Mechanical Interface: Single-Width Module.

### Electrical

- **XMC PCIe bus interface (P15 and P16)**
  - One 114-pin male connector (Samtec ASP-103614-05 or equivalent).
  - P15 primary XMC connector:
    - 8 differential pairs (PCIe x4 standard, Serial RapidIO, 10-Gigabit Ethernet, or Xilinx Aurora). JTAG.
    - System Management (XMC provides hardware definition information read by an external controller using IPMI commands and 12C serial bus transactions.)
    - 3.3V power: 4 pins at 1A/pen.
    - 3.3V auxiliary power: 1 pin, powers volatile memory to store the bitstream encryption key.
    - Variable power (5V or 12V): 8 pins at 1A per pin.
  - P16 XMC connector:
    - 8 differential pairs (PCIe, Serial RapidIO, or Xilinx Aurora).
    - 17 LVDS pairs or 34 SelectI/O signals (differential pairs grouped per VITA 46.0 X38s).
    - 2 global clock pairs.
    - Vcco pins are powered by 2.5V and support the 2.5V I/O standards.
  - P4 PMC rear I/O connector:
    - 64-pin female receptacle header (AMP 120527-1 or equivalent).
    - 64 I/O connections (30 LVDS pairs plus two global clocks).
    - Vcco pins powered by 2.5V and support the 2.5V I/O standards.

### Environmental

- **Operating temperature**
  - XMC-7A200-LF: -40 to 55°C.
- **Storage temperature**
  - -55 to 125°C.
- **Relative humidity**
  - 5 to 95% non-condensing.

### Ordering Information

- **NOTE:** XMC-7KA-EDK is required to configure FPGA.

### Accessories

- **AXM-A75**
  - 16 analog inputs, 8 analog outputs, and 16 digital I/O
- **AXM-A30**
  - 2 analog input 100MHz 16-bit A/D channels.
- **AXM-D02**
  - 30 RS485 differential I/O channels.
- **AXM-D03**
  - 16 CMOS and 22 RS485 differential I/O channels.
- **AXM-D04**
  - 30 LVDS I/O channels.
- **AXM-??**
  - Custom I/O configurations available, call factory

### Software

- **For more information, see www.acromag.com.**

- **XMC-7KA-EDK**
  - Engineering Design Kit (one kit required)

- **PMCSW-API-VXW**
  - VxWorks® 32-bit software support package

- **PCISW-API-WIN**
  - Windows® DLL software support package

- **PCISW-API-LNX**
  - Linux® support (website download only)