PCI-9118/L Series

16-CH 12 Bit Up to 333 kS/s Analog Input Cards









Introduction

ADLINK's PCI-9118/L series are high-performance data acquisition cards that are simplified versions of the phased-out PCI-9118. The PCI-9118/L series provides full compatible functionality with the PCI-9118 series except for the analog output functions. The PCI-9118DG/L and PCI-9118HG/L feature 12-bit resolution, with sampling rate up to 333 kS/s.

The 256-location channel gain queues on PCI-9118/L series cards allow high-speed data acquisition with different gains on each channel and non-sequential order of automatic analog input scanning capability. The onboard 1 k-sample A/D FIFO ensures reliable high-speed data acquisition under Windows operating systems. The data can be transferred through bus-mastering DMA with gap-free, continuous high throughput; even for a large amount of data.

ADLINK PCI-9118/L series analog input cards deliver cost-effective and reliable data acquisition capabilities, and are ideal for a broad variety of applications.

Features

- Supports a 32-bit 5 V PCI bus
- 12-bit A/D resolution
- Up to 333 kS/s sampling rate
- 16 single-ended or 8 differential inputs
- 256-configuration channel gain queue
- Onboard I k-sample A/D FIFO
- Bipolar or Unipolar analog input ranges
- Programmable gains:
 - x1, x2, x4, x8 (PCI-9118DG/L)
 - x1, x10, x100 (PCI-9118HG/L)
- Bus-mastering DMA for analog inputs
- 4-CH TTL digital inputs and 4-CH TTL digital outputs
- Compact, half-size PCB

Operating Systems

- Windows 7/Vista/XP/2000/2003 Server
- Linux

■ Recommended Software

- AD-Logger
- $\bullet \ VB.NET/VC.NET/VB/VC++/BCB/Delphi\\$
- DAQBench

■ Driver Support

- DAQPilot for LabVIEW $^{\text{\tiny TM}}$
- DAQ-MTLB for MATLAB®
- PCIS-DASK for Windows
- PCIS-DASK/X for Linux

Specifications

Analog Input

- Number of channels
- · 16 single-ended or 8 differential
- Channel gain queue size: 256 configurations
- Resolution
 - · 12 hits
- Conversion time
 - · 3 µs
- Maximum sampling rate
 - · 333 kS/s
- Input signal ranges: (software programmable)

Device	Input Range			
	Gain	Bipolar	Unipolar	
PCI-9118DG/L	- 1	±5 V	0 to 10 V	
	2	±2.5 V	0 to 5 V	
	4	±1.25 V	0 to 2.5 V	
	8	±0.625 V	0 to 1.25 V	
PCI-9118HG/L	- 1	±5 V	0 to 10 V	
	10	±0.5 V	0 to 1 V	
	100	±0.05 V	0 to 0.1 V	

Accuracy

Device	Gain	Accuracy
PCI-9118DG/L	I	0.008% of FSR ± 1 LSB
	2	0.01% of FSR ± 1 LSB
	4	0.02% of FSR ± 1 LSB
	8	0.04% of FSR ± 1 LSB
PCI-9118HG/L	I	0.008% of FSR ± 1 LSB
	10	0.01% of FSR ± 1 LSB
	100	0.02% of FSR ± 1 LSB

- Input coupling: DC
- Overvoltage protection: continuous ±35 V
- Input impedance: I GΩ
- Trigger modes software, pacer, and external trigger (5 V/TTL compatible)
- FIFO buffer size: I k samples
- Data transfers:
 - polling, interrupt, bus-mastering DMA

Digital I/O

- Number of channels: 4 inputs and 4 outputs
- Compatibility: 5 V/TTL
- Data transfers: programmed I/O

General Specifications

- I/O connector: 50-pin SCSI-II female
- Operating temperature: 0°C to 55°C
- Storage temperature: -20°C to 80°C
- Relative humidity: 5% to 95%, non-condensing

Power requirements

Device	+5 V
PCI-9118DG/L, PCI-9118HG/L	450 mA typical

Dimensions (not including connectors)173 mm x 107 mm

Ordering Information

■ PCI-9118DG/L

16-CH 12-Bit 333 kS/s Normal-GainAnalog Input Card

■ PCI-9118HG/L

16-CH 12-Bit 333 kS/s High-Gain Analog Input Card

Terminal Boards & Cables

■ DIN-50S-01

Terminal Board with One 50-pin SCSI-II Connector and DIN-Rail Mounting (Cables are not included.)

ACL-10250-1

50-pin SCSI-II cable (mating with AMP-787082-5), I M

Pin Assignment

U_CMMD	1	26	(AIH0) AI0
Al8 (AIL0)	2	27	(AIH1) AI1
AI9 (AIL1)	3	28	(AIH2) AI2
AI10 (AIL2)	4	29	(AIH3) AI3
AI11 (AIL3)	5	30	(AIH4) AI4
AI12 (AIL4)	6	31	(AIH5) AI5
AI13 (AIL5)	7	32	(AIH6) AI6
AI14 (AIL6)	8	33	(AIH7) AI7
AI15 (AIL7)	9	34	AGND
N/C	10	35	N/C
N/C	11	36	N/C
N/C	12	37	N/C
+15Vout	13	38	-15Vout
DGND	14	39	ADGAIN2
DI1	15	40	DI0
DI3	16	41	DI2
DO1	17	42	DO0
DO3	18	43	DO2
DOSTB	19	44	EXTTRG
TGOUT	20	45	SSHO
ADCHN3	21	46	TGIN
ADCHN5	22	47	ADCHN4
ADCHN7	23	48	ADCHN6
Vcc	24	49	Vcc
DGND	25	50	DGND

^{*} For more information on mating cables, please refer to P2-61/62.